

# The Read-Out System of the ALICE Pixel Detector

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*CERN-EP/ED*

*for the ALICE Pixel Detector  
Collaboration*

**PIXEL 2002,**  
**Carmel, California, September 9, 2002**

# Presentation scope

- Read-out Architecture
- ASIC development and test systems
- Physical implementation

# ALICE Pixel Detector

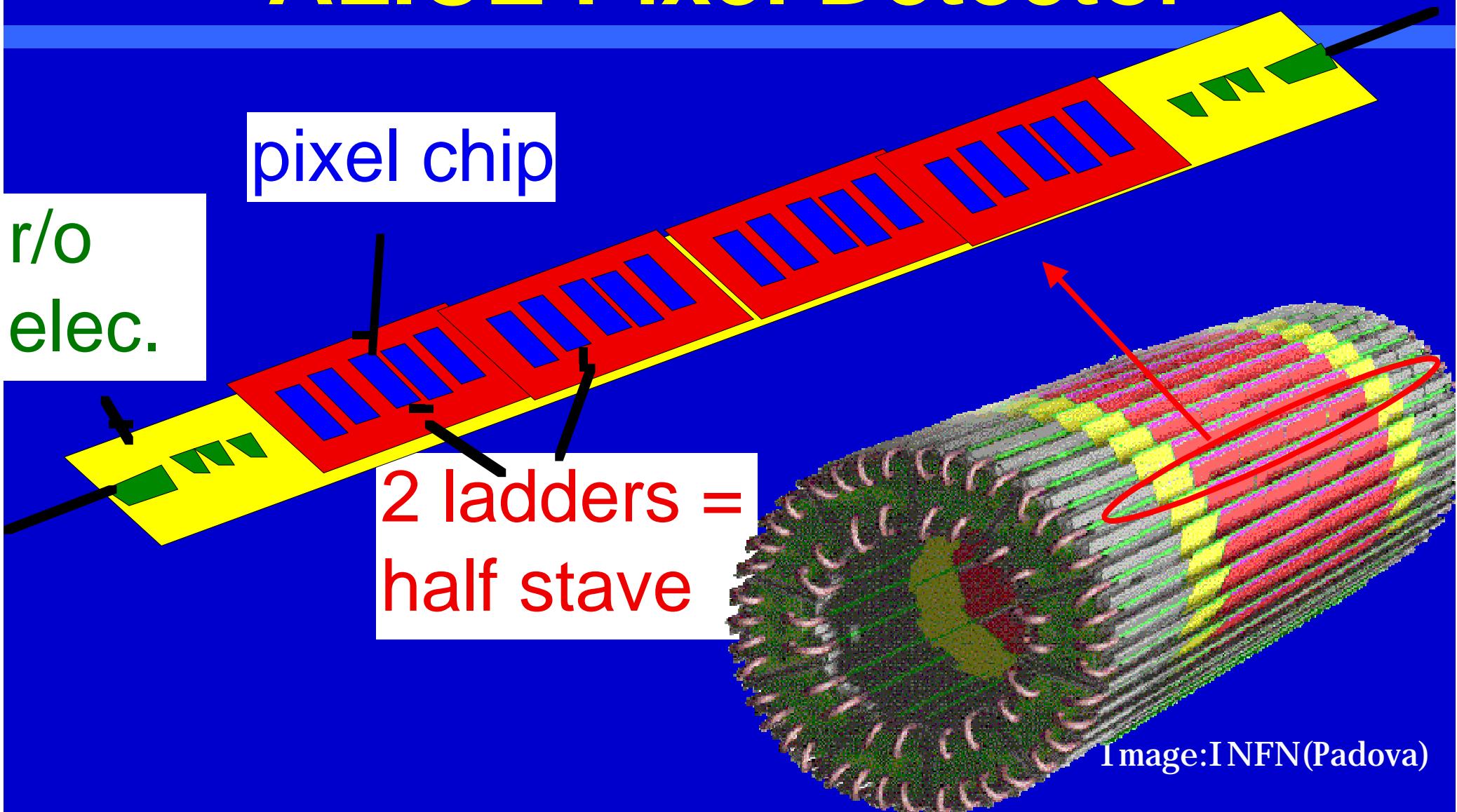
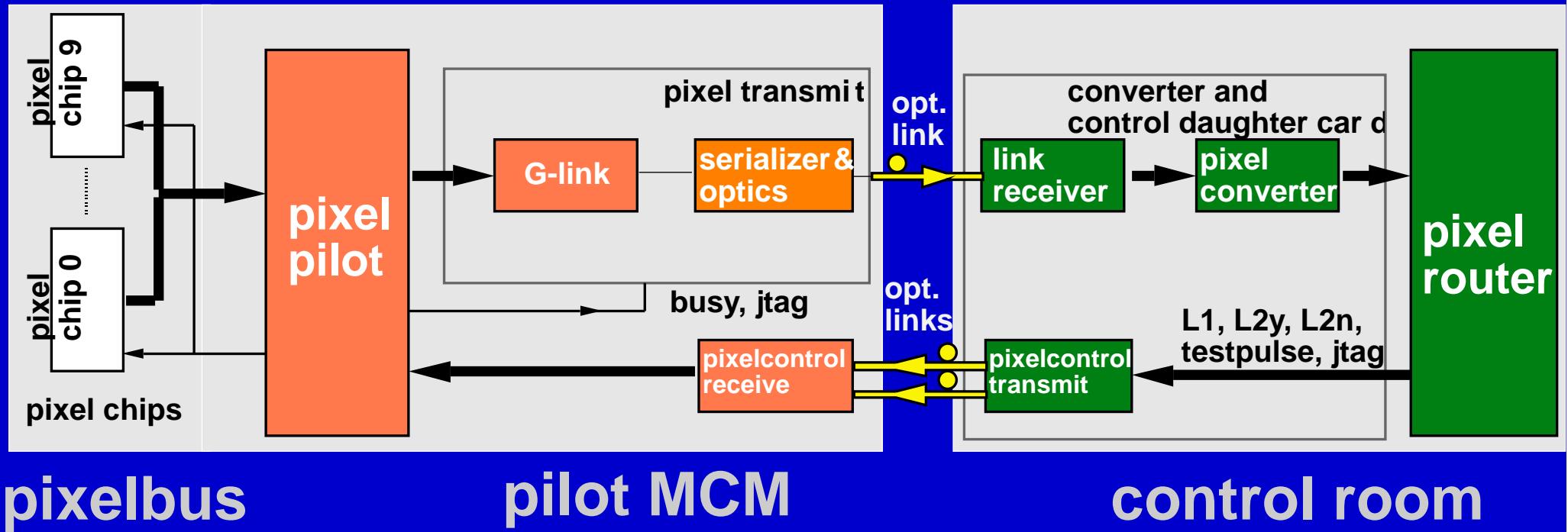


Image:INFN(Padova)

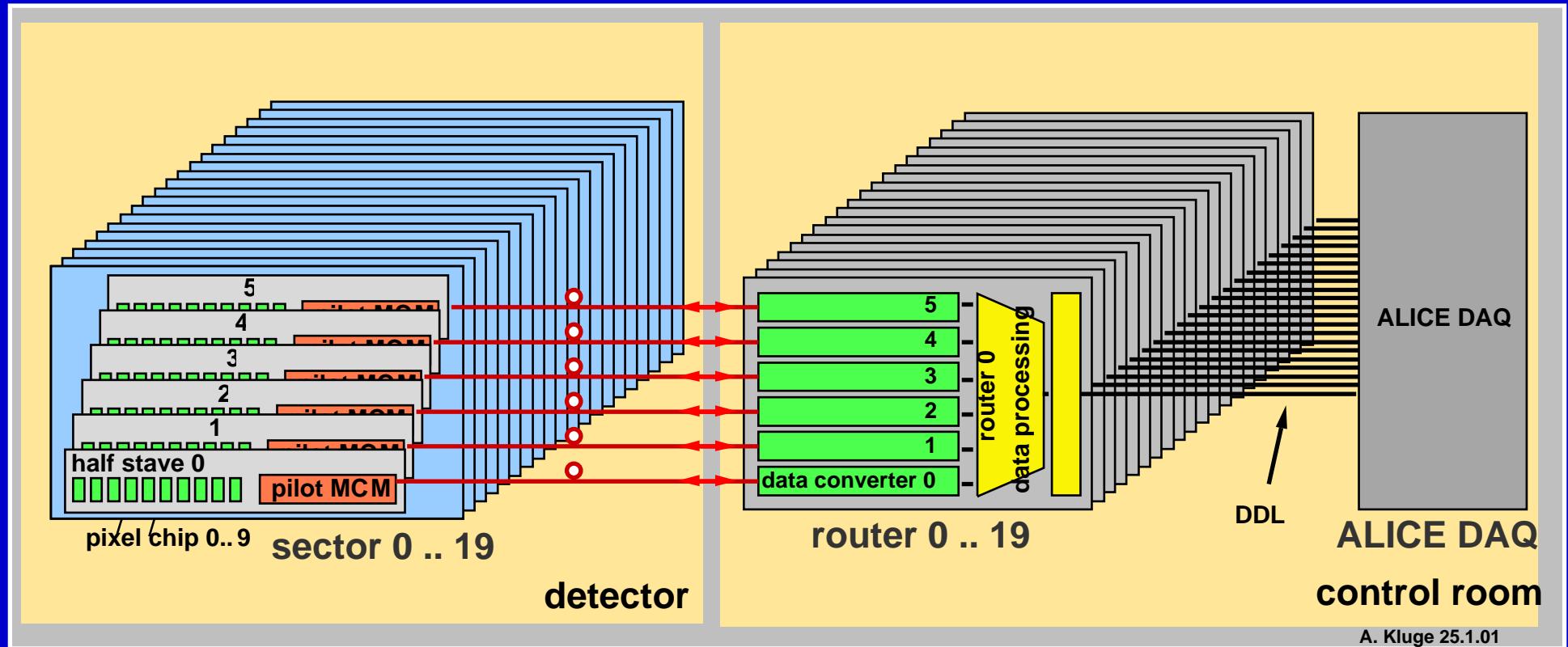
# System Requirements

- L1 after 6  $\mu$ s, L2 after 100  $\mu$ s
- L1 rate 1 kHz, L2 rate 40- 800Hz
- Readout upon L2
  - ~ 1 GB/s raw data
- Small physical implementation
- 10 MHz system clock
- Configurable by JTAG
- Radiation: < 500 krad,  
neutron flux  $3 \times 10^{11} \text{cm}^{-2} (10\text{y})$
- SEU safe

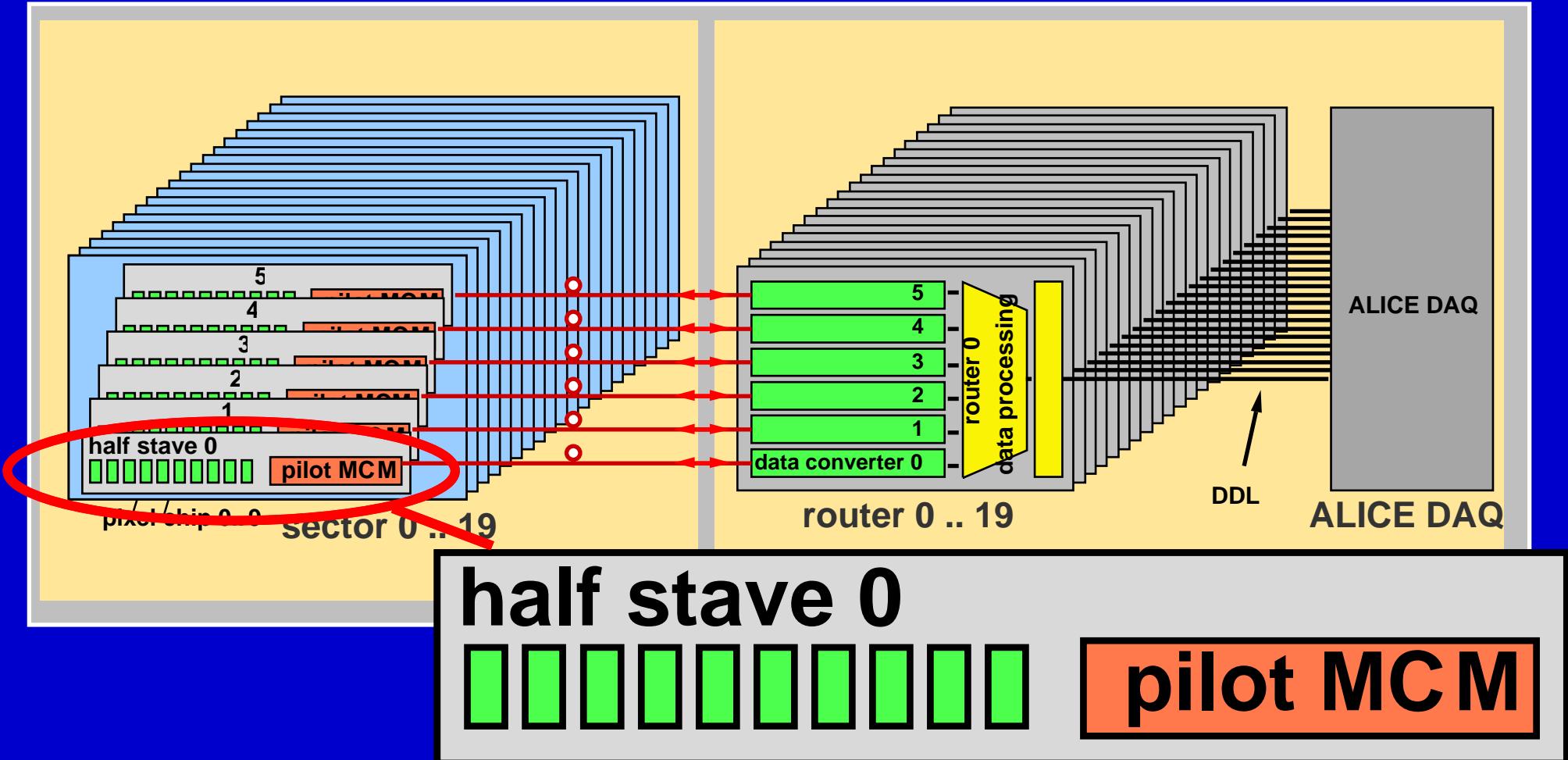
# OPS implementation



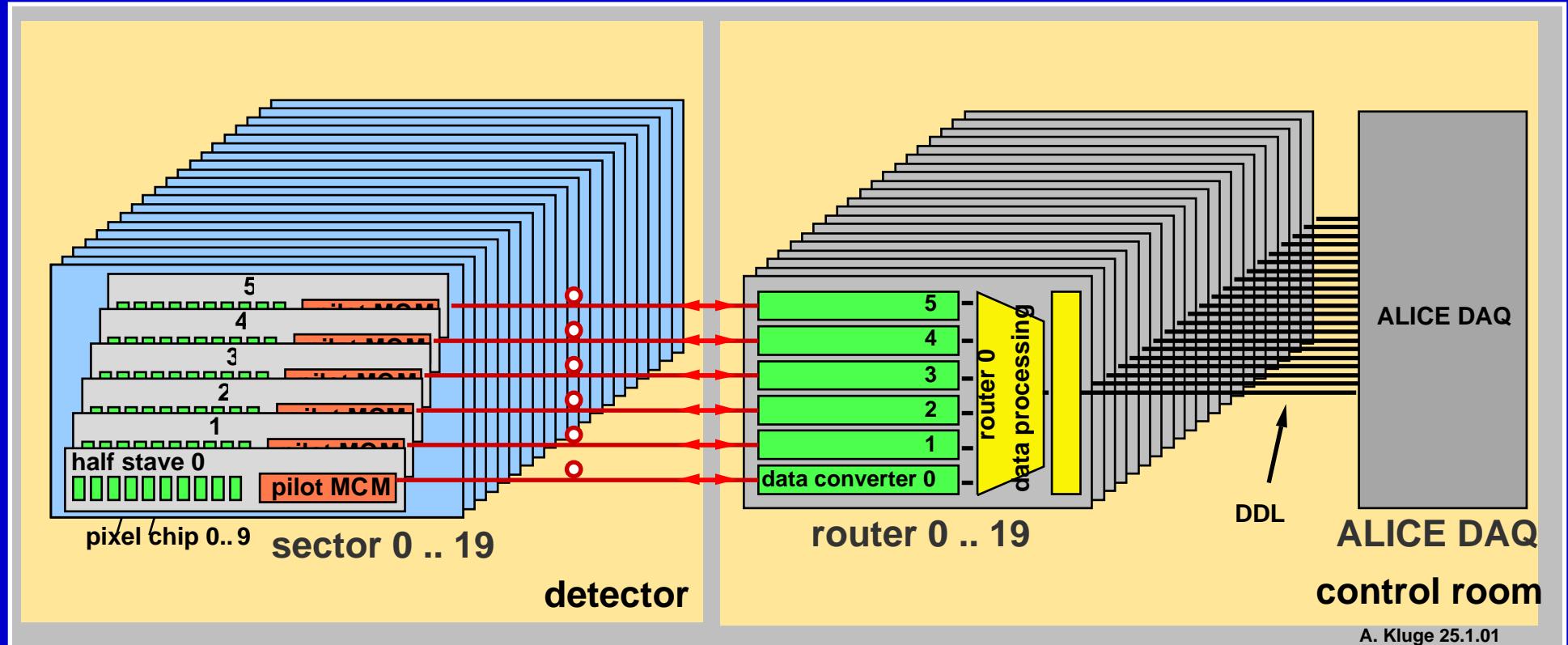
# OPS overview



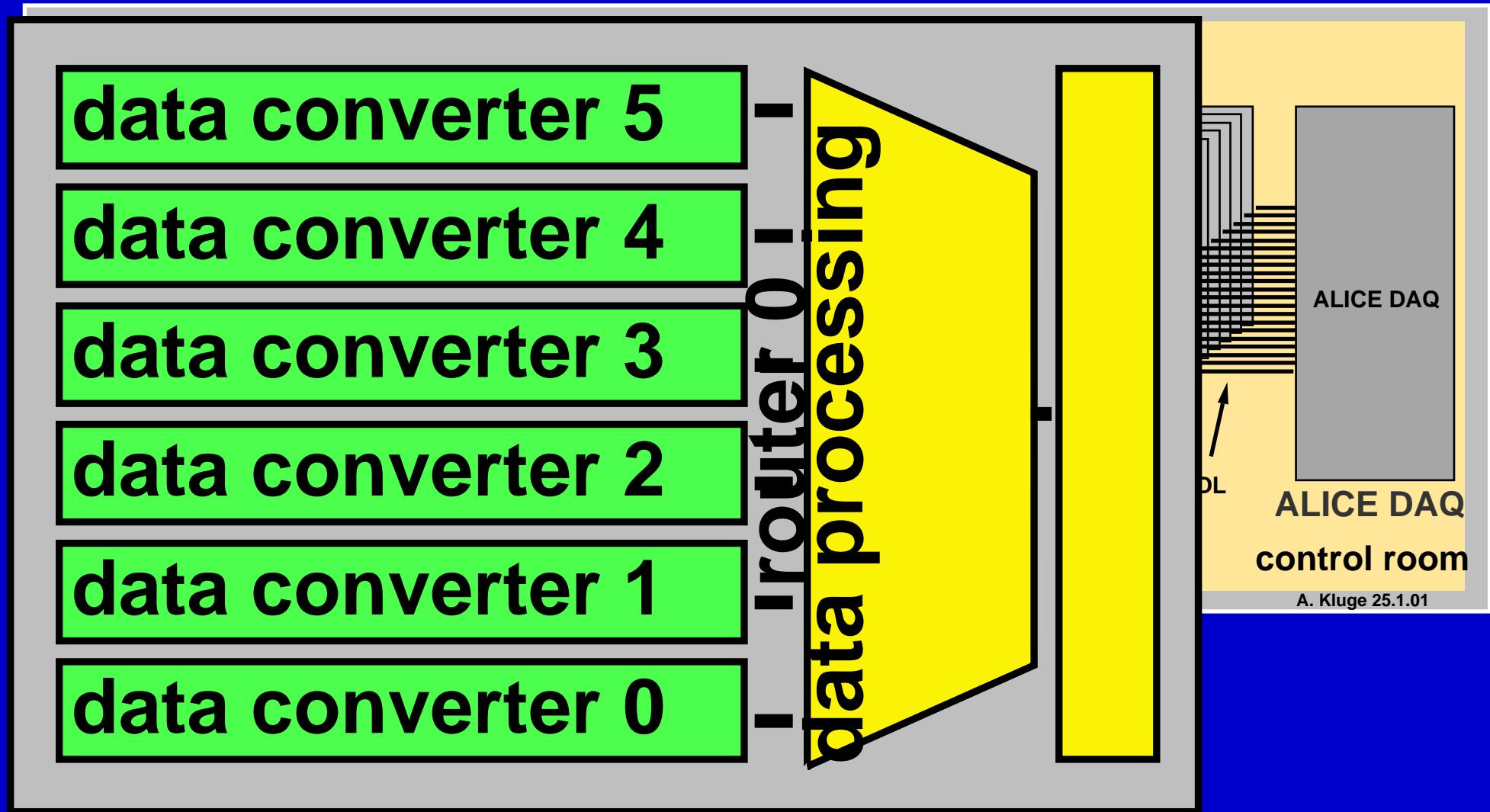
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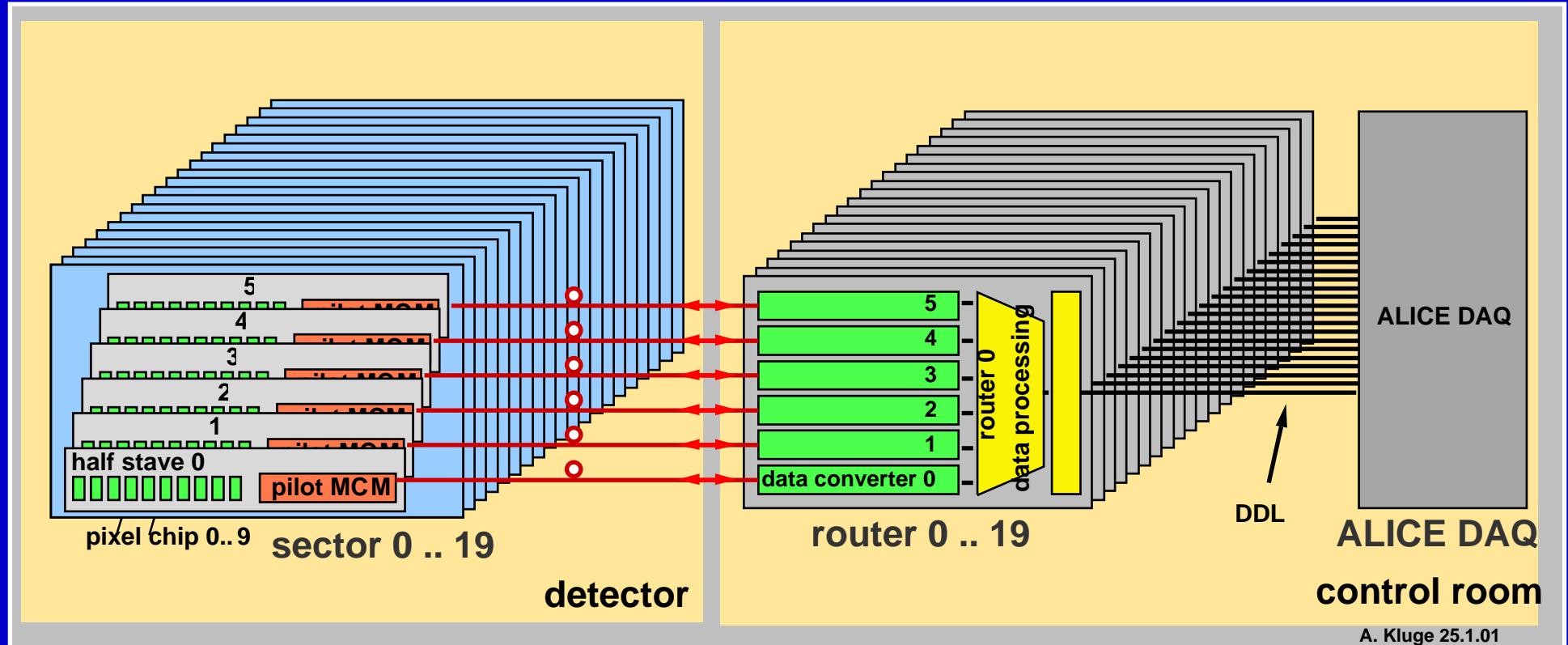
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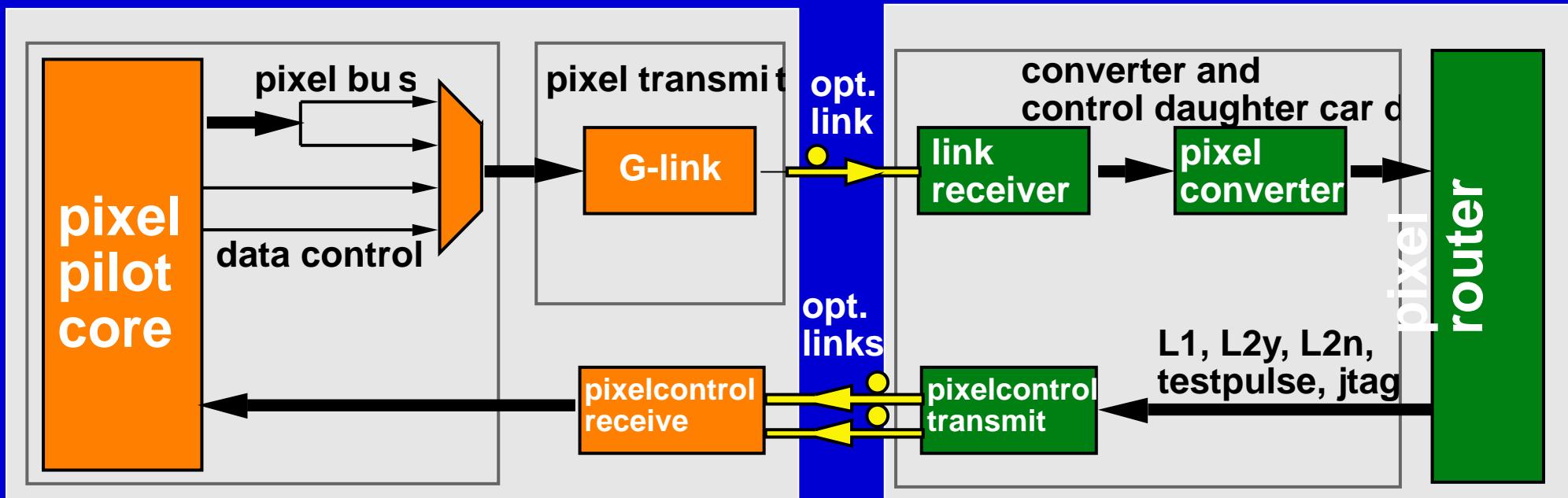
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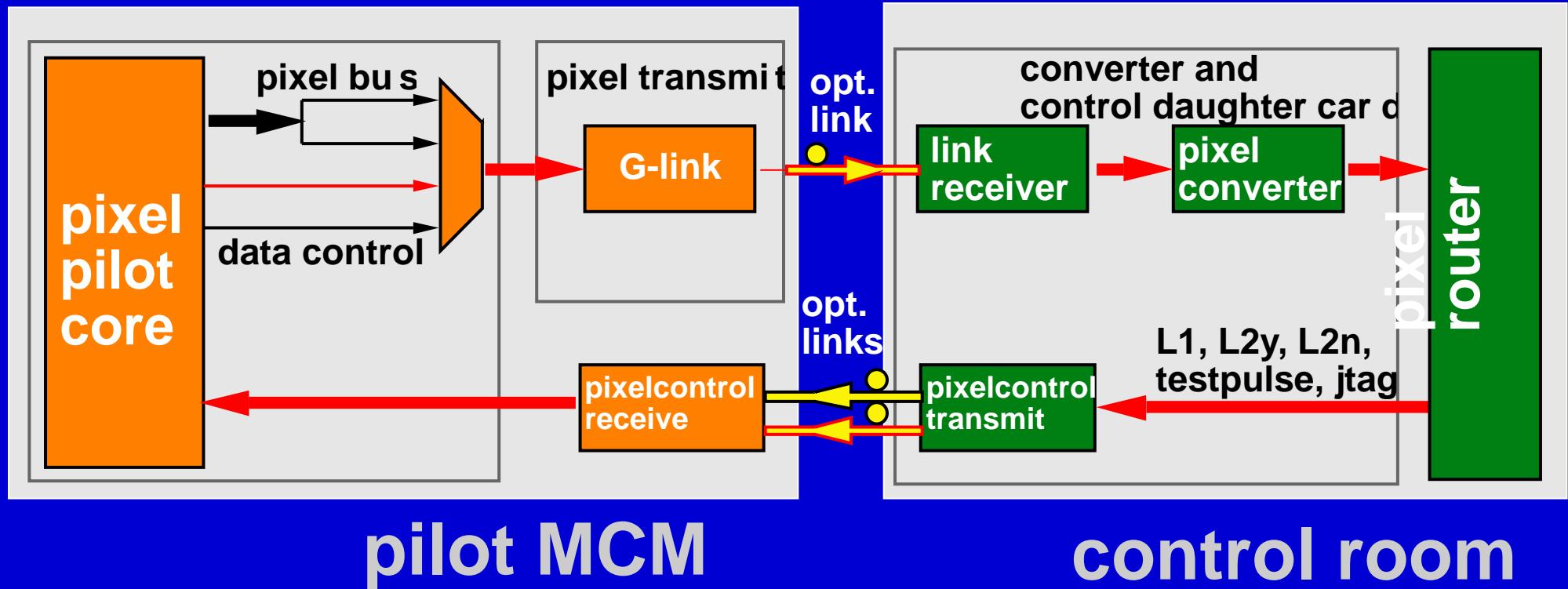


pilot MCM

control room

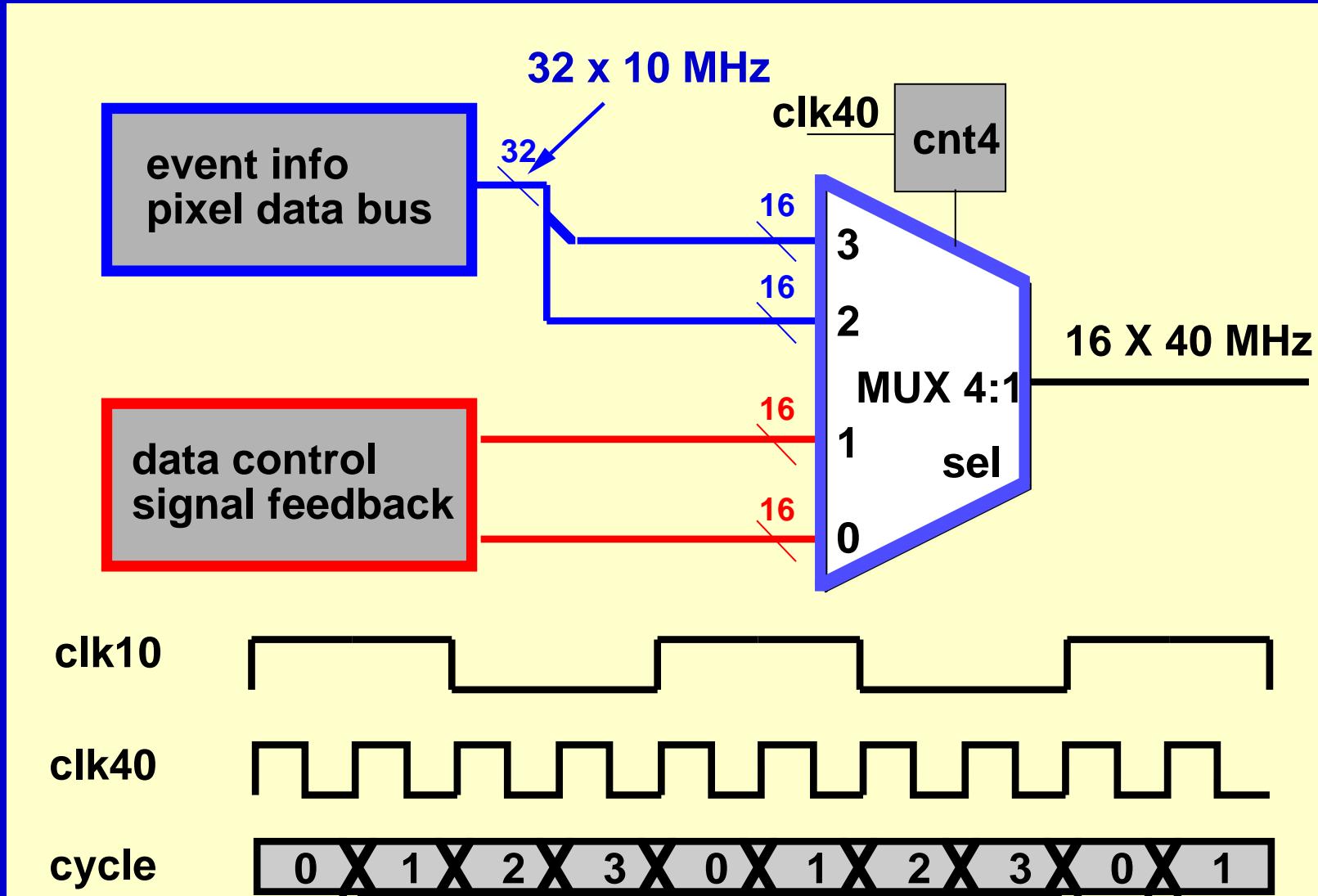
A. Kluge 28.8.01

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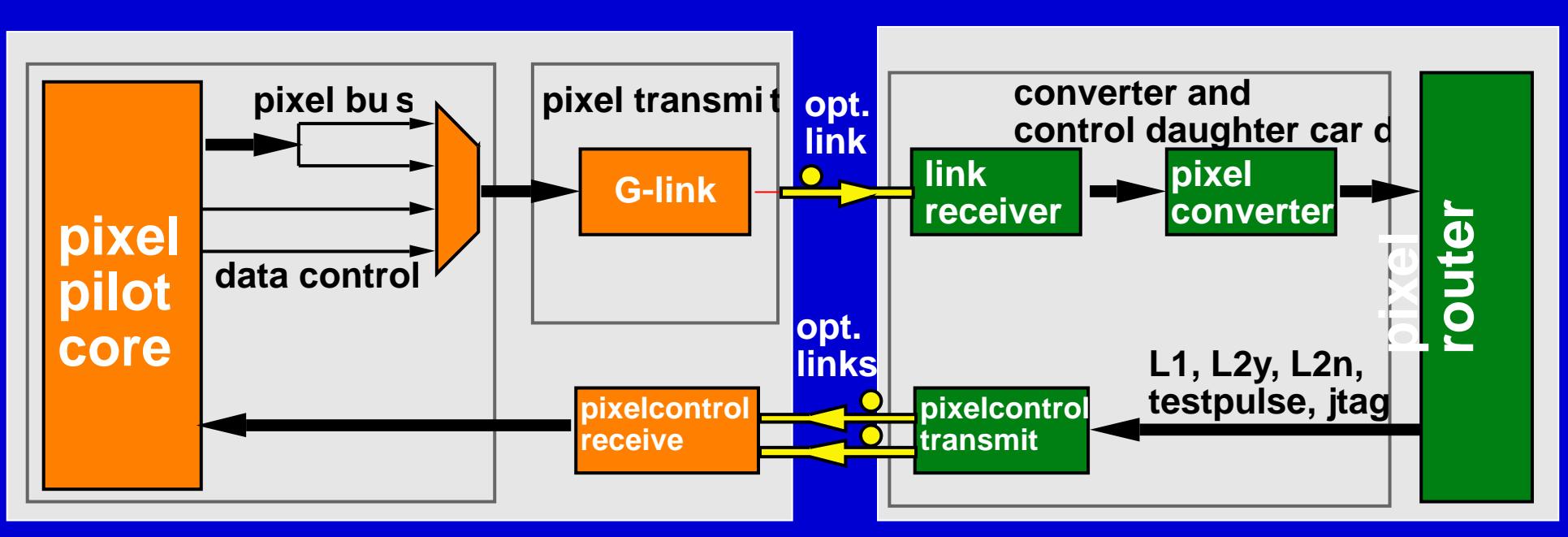


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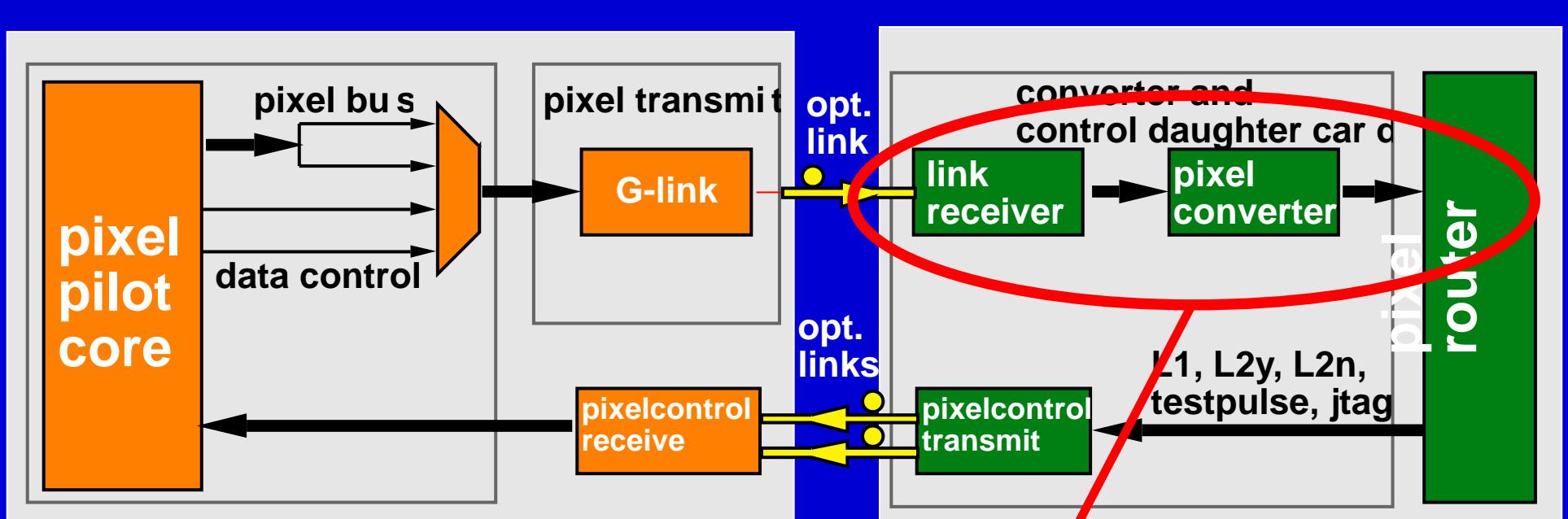
# OPS transmission principle



# Link receiver / data converter



# Link receiver / data converter



pilot MCM

control room

A. Kluge 28.8.01

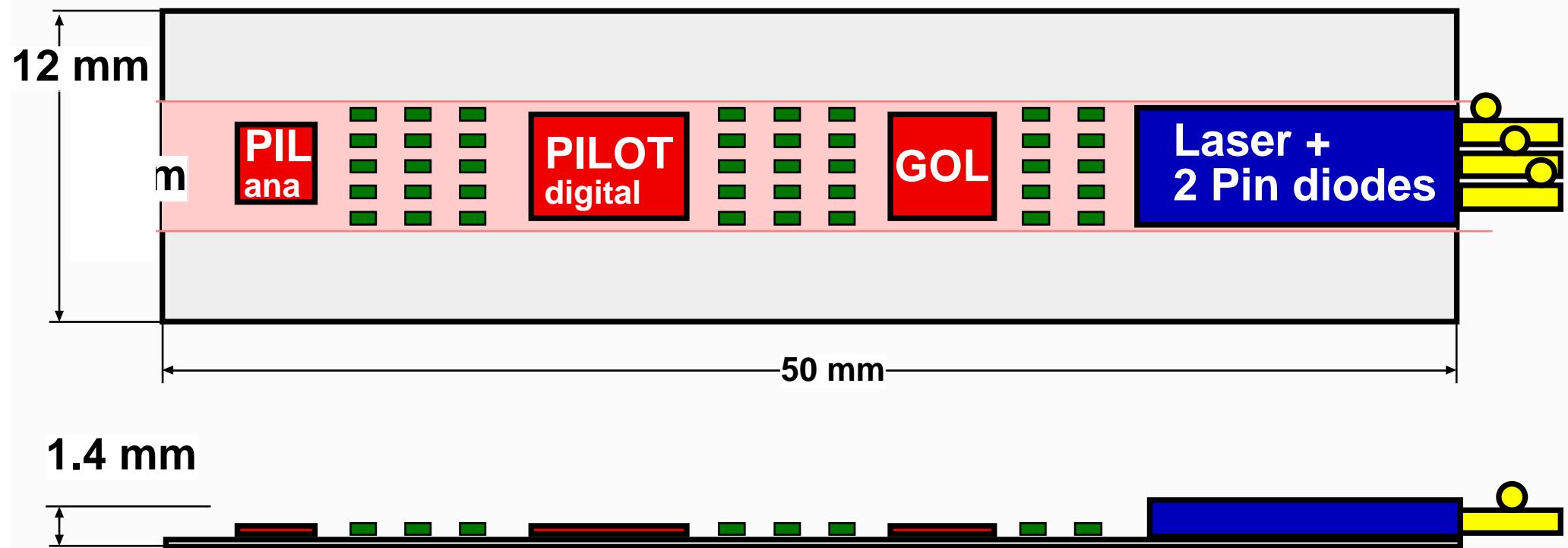


# ASIC Development

Sept 9, 2002

A. Kluge

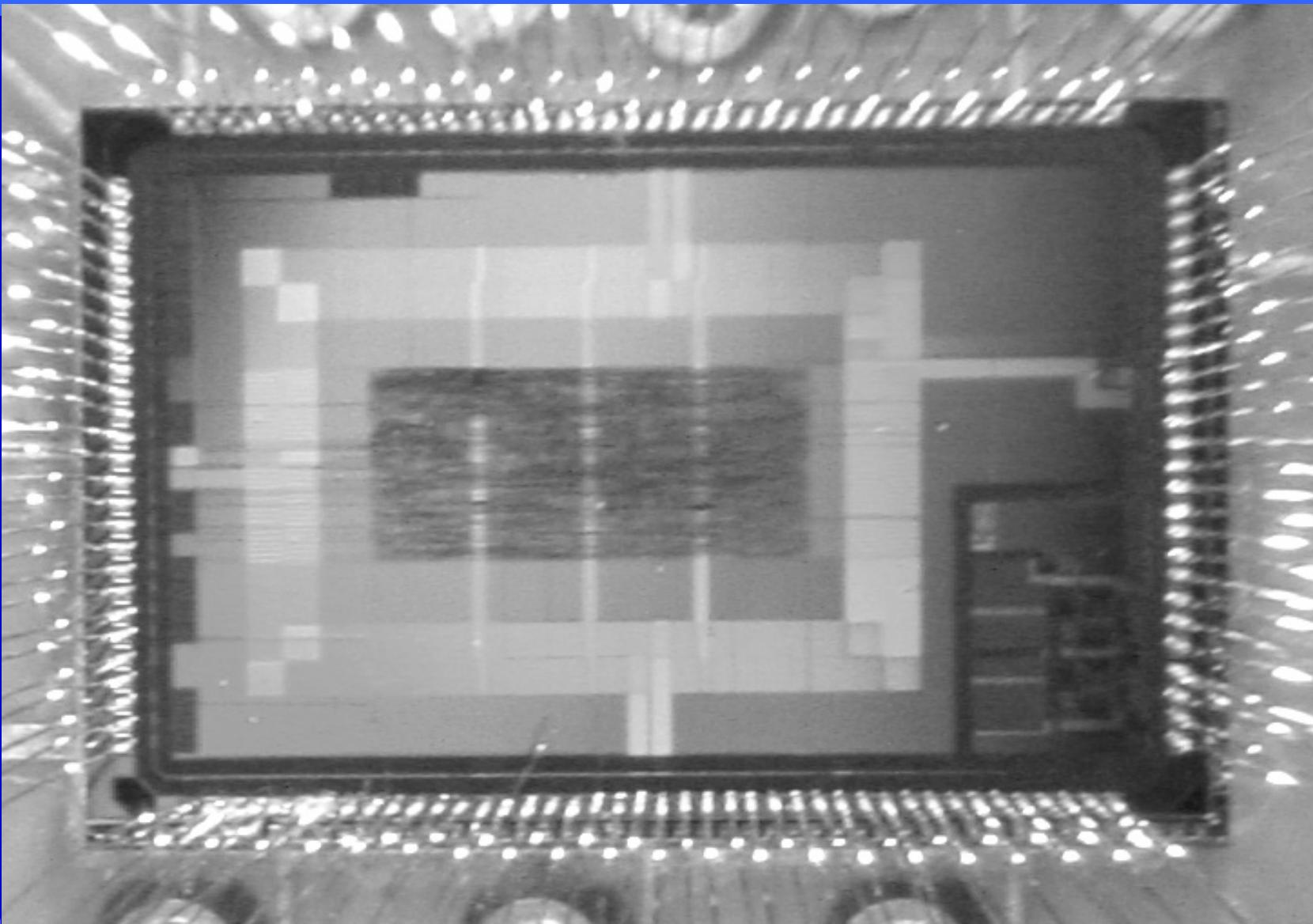
# Pilot MCM



# ASIC implementation

- IBM 0.25  $\mu\text{m}$  ASIC designs (rad tolerant design)
- No on detector data processing, no memory on detector
- Use of already developed Glink chip GOL
- Only 3 optical connections
  - No GND loops

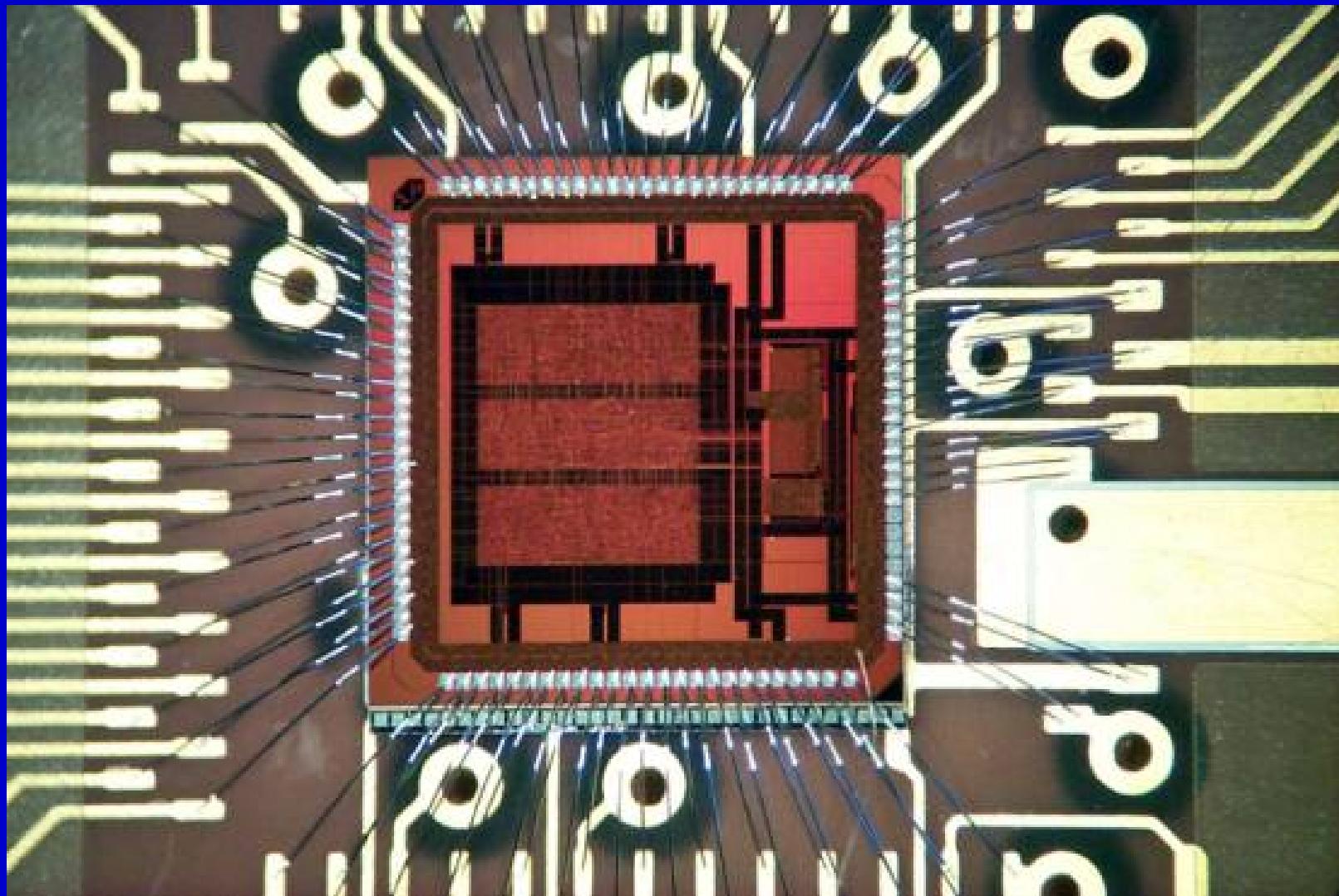
# Digital Pilot chip



Sept 9, 2002

A. Kluge

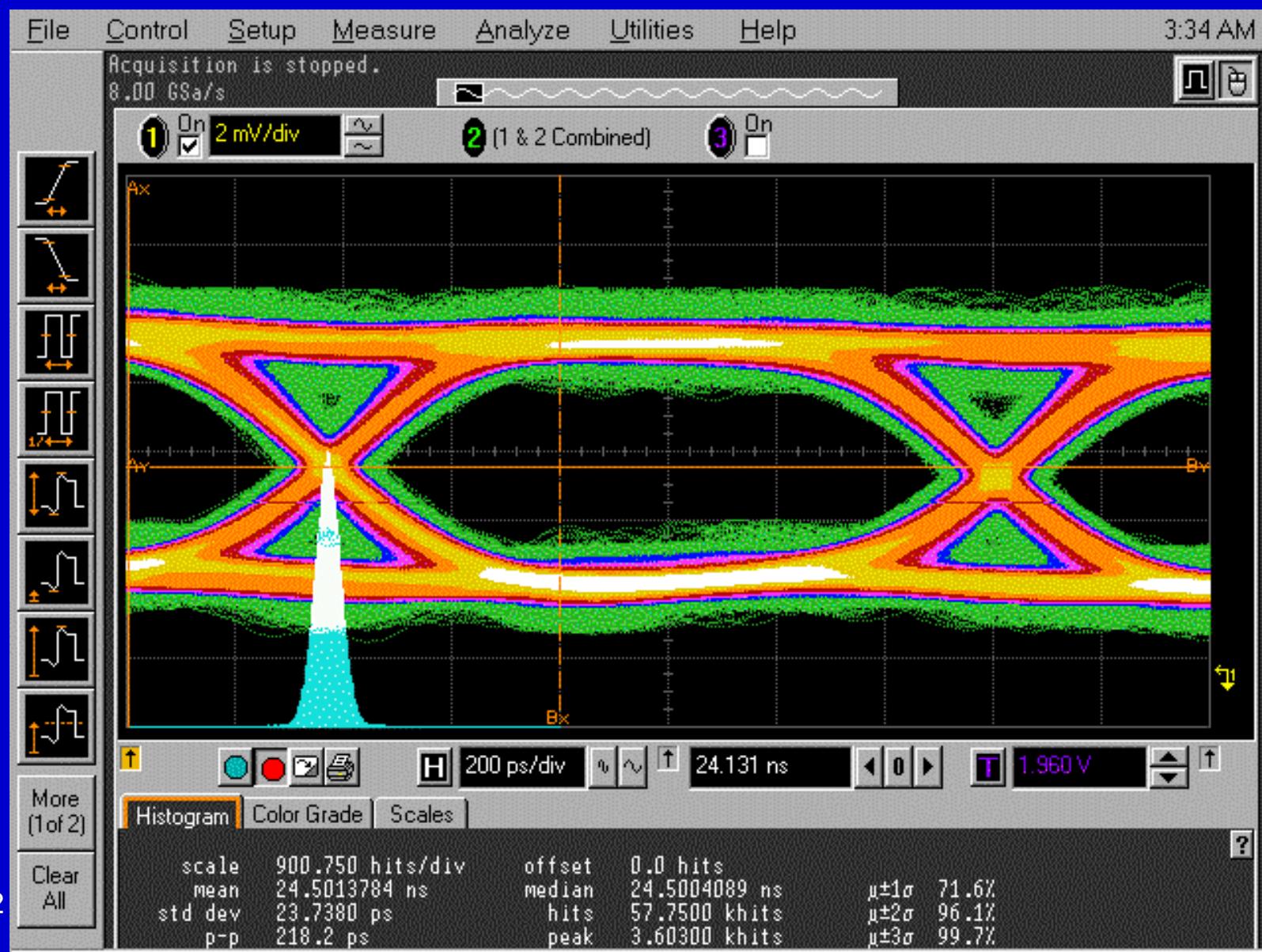
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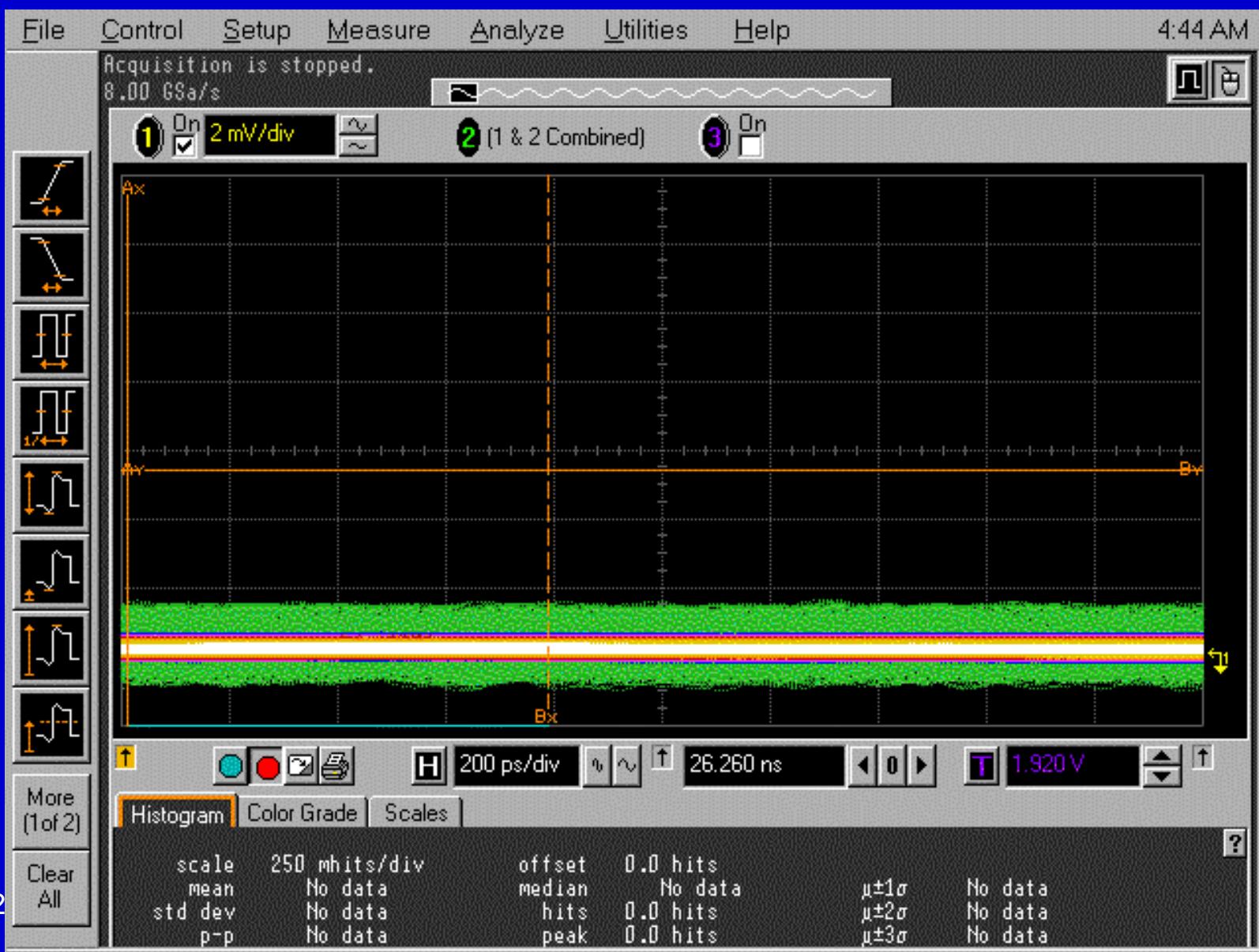
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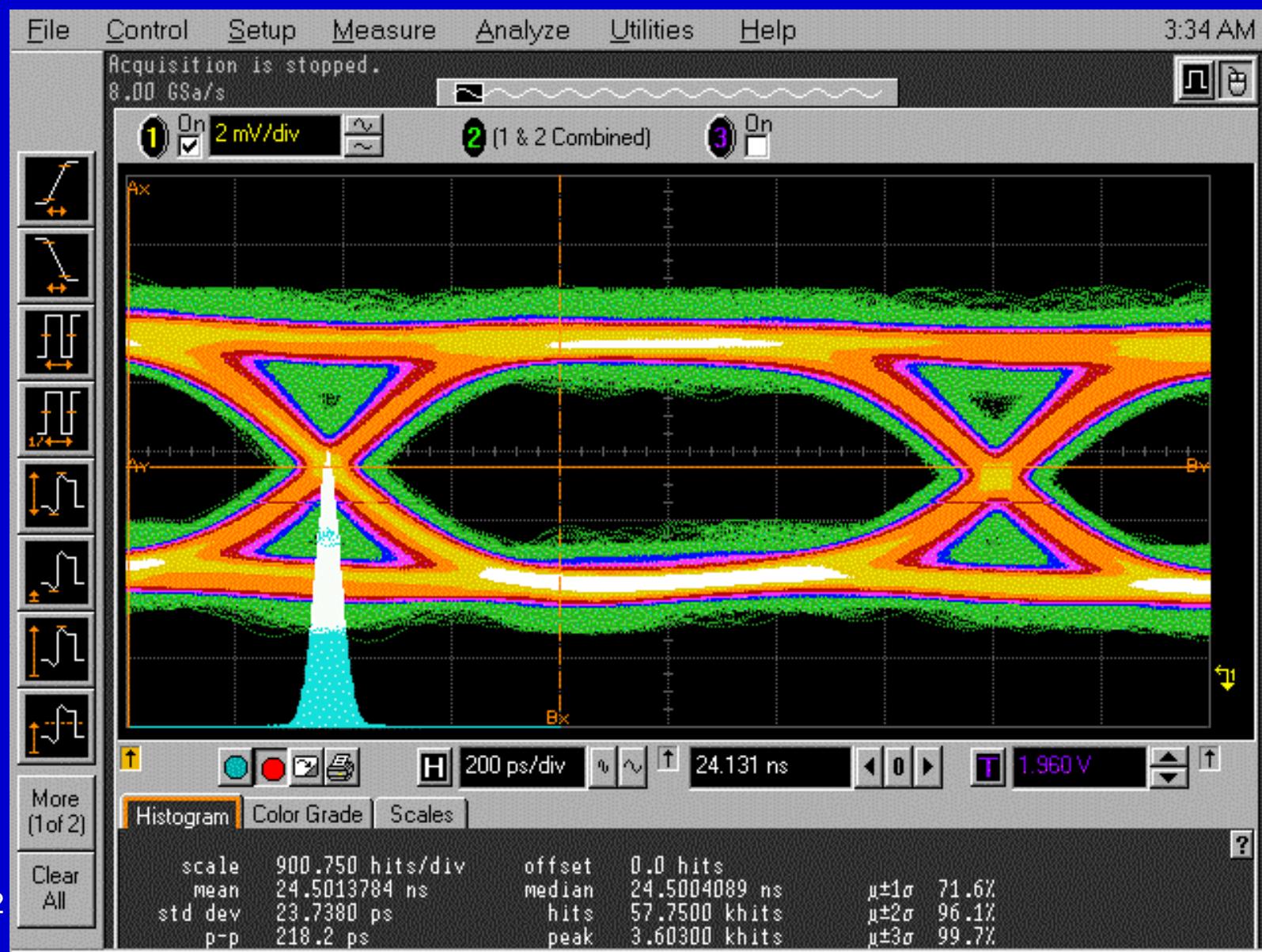
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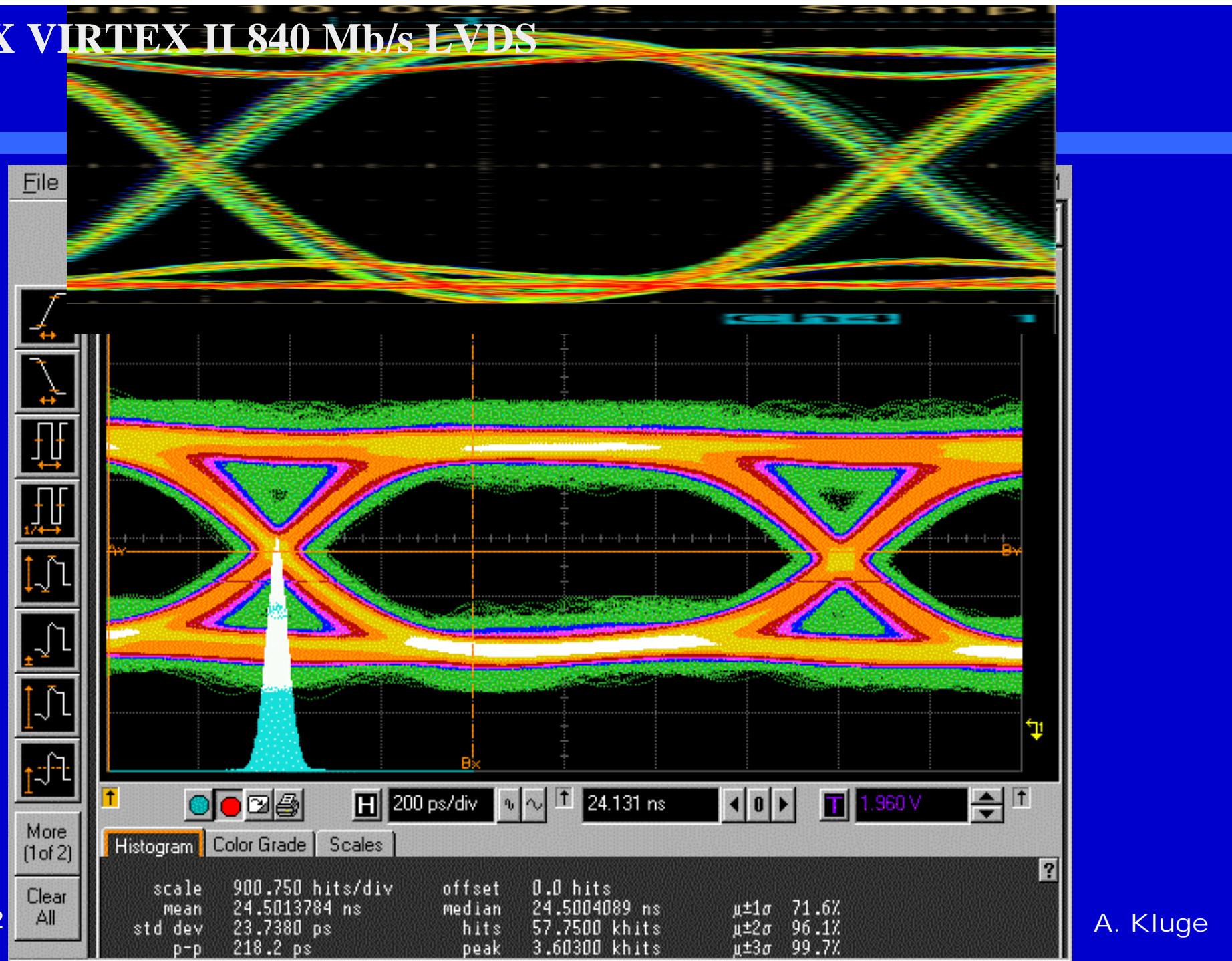
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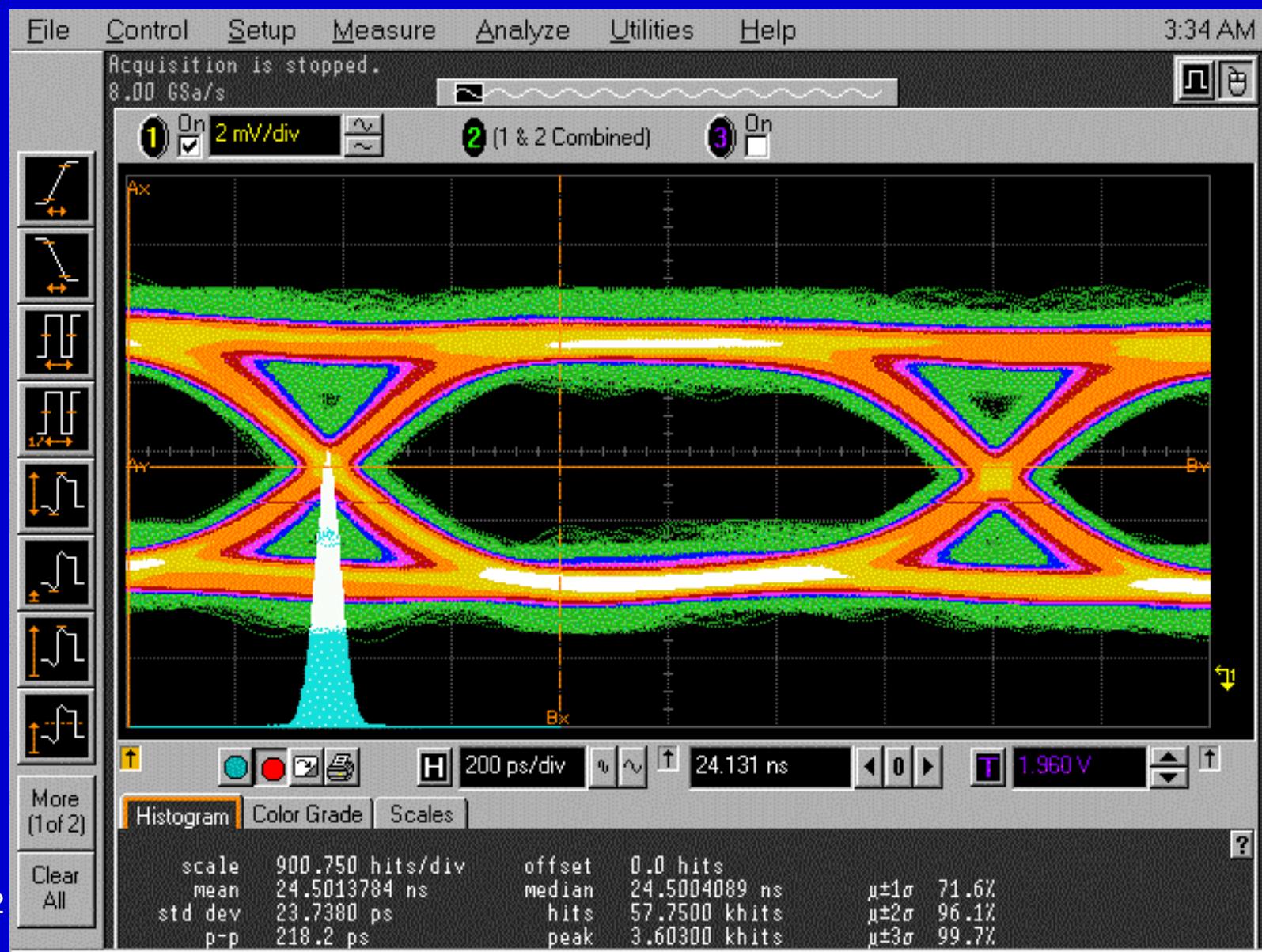
# XILINX VIRTEX II 840 Mb/s LVDS



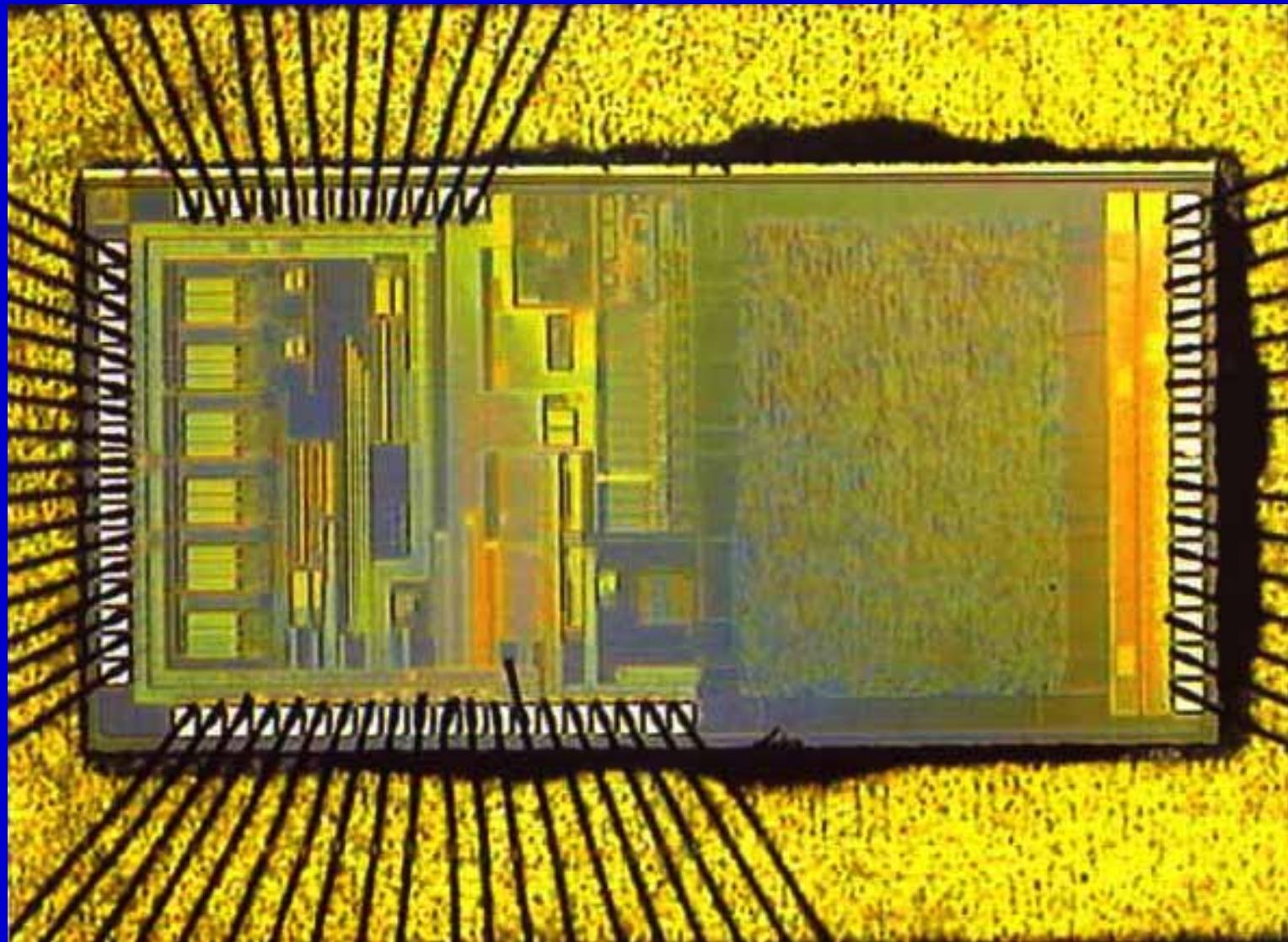
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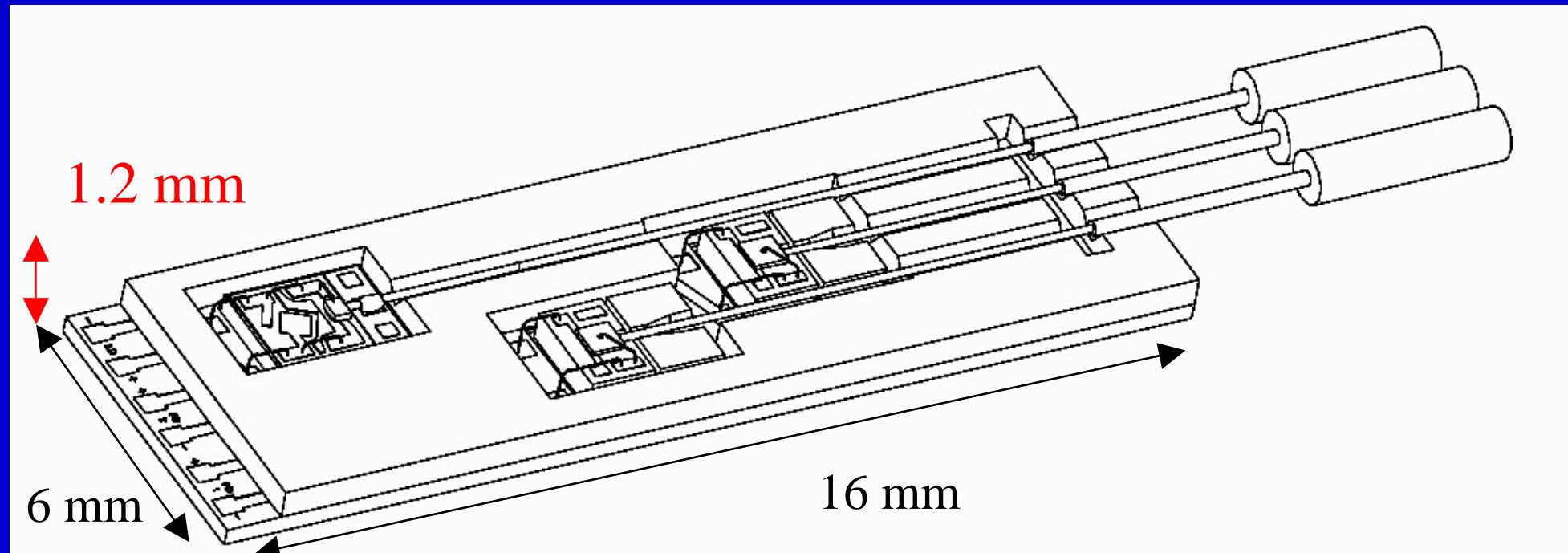
# Analog Pilot chip



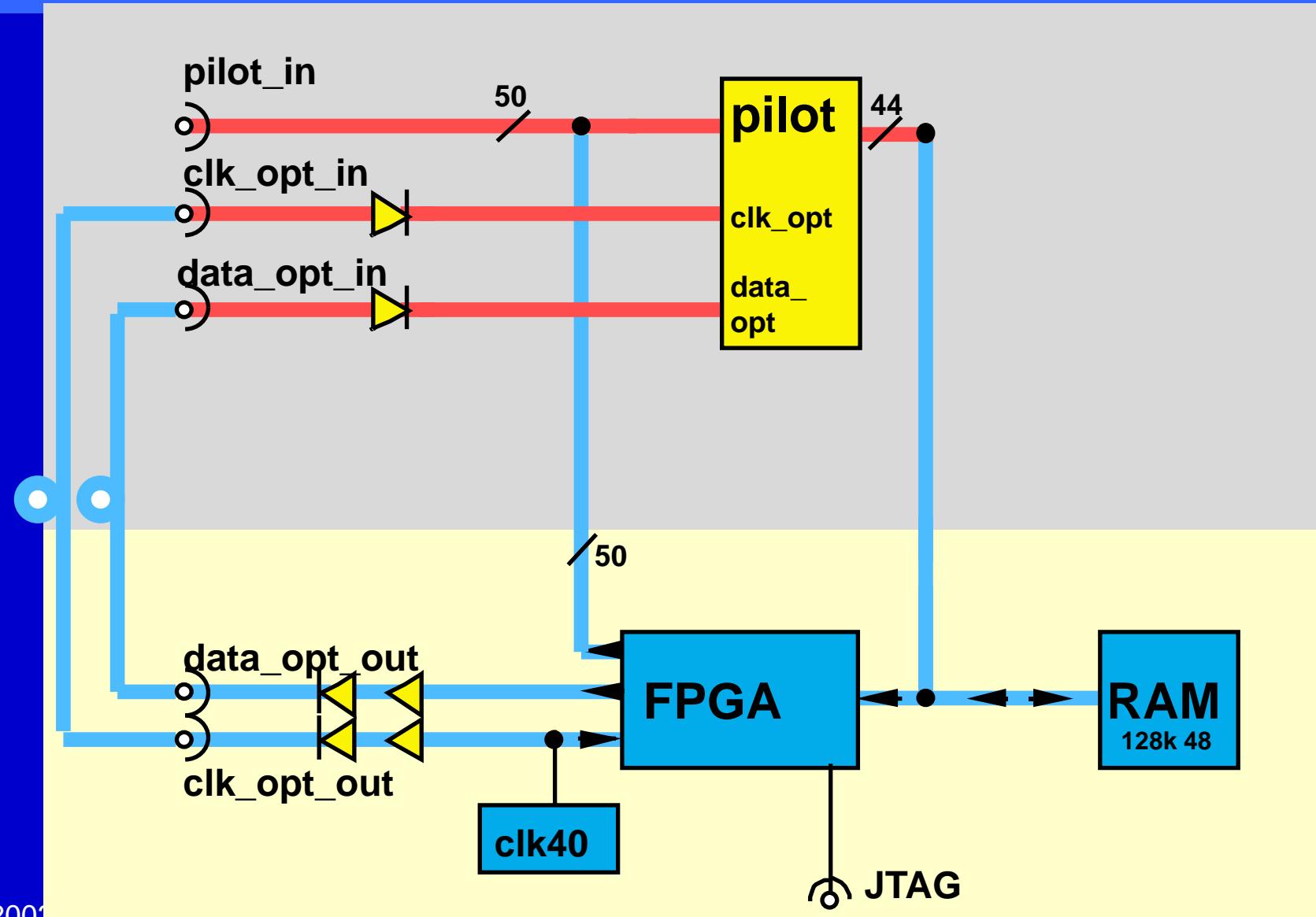
Sept 9, 2002

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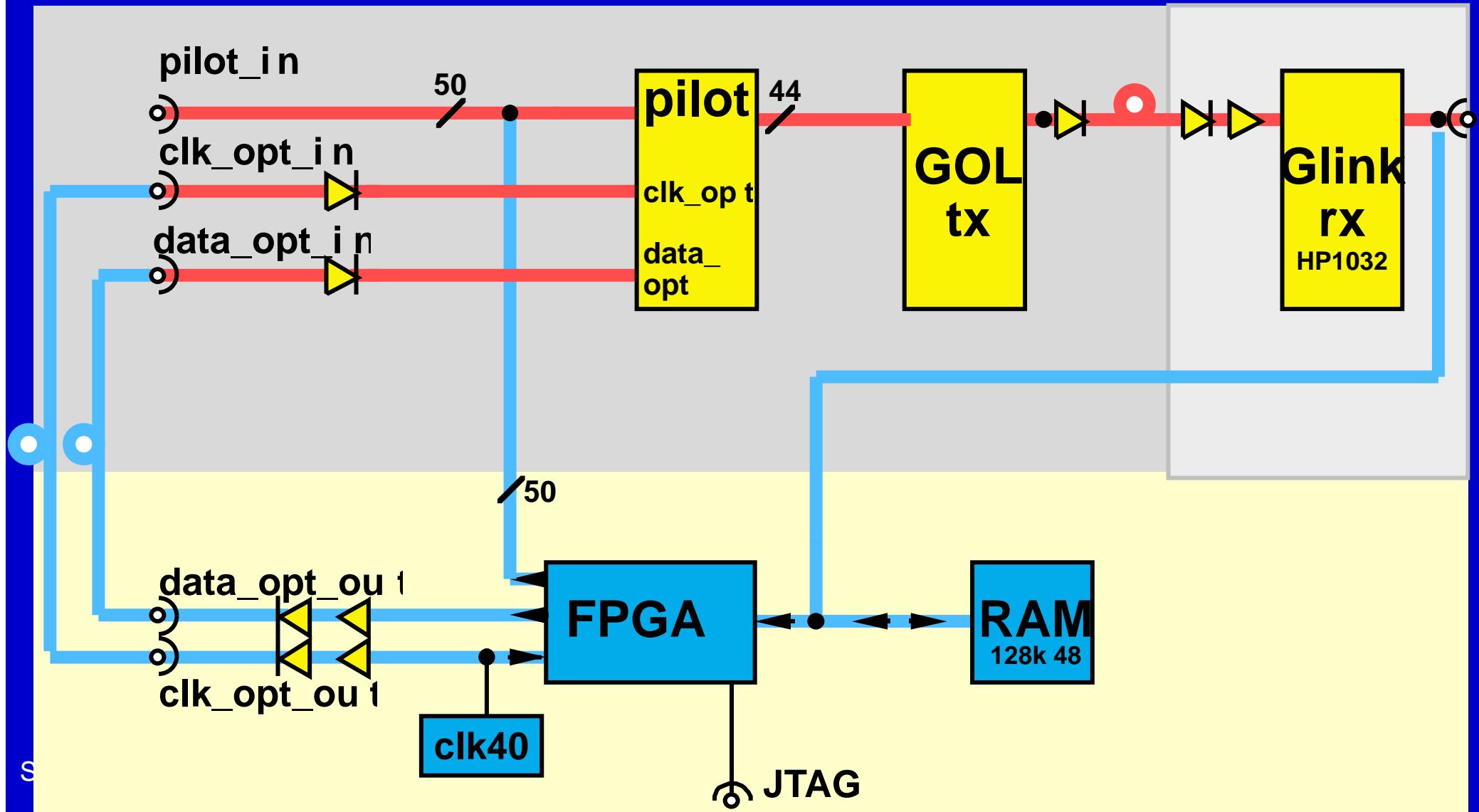
# Optical package



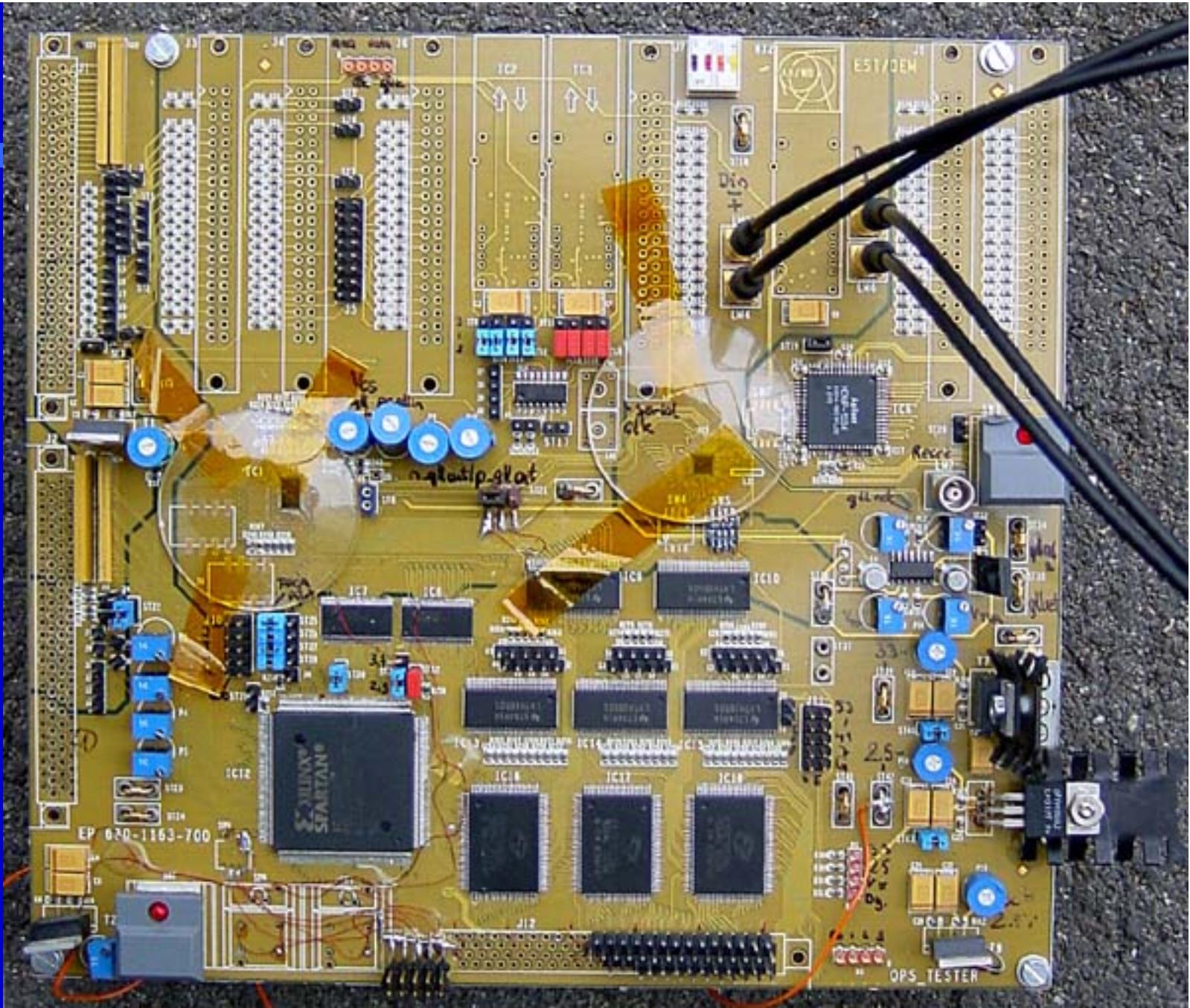
# OPS Test system



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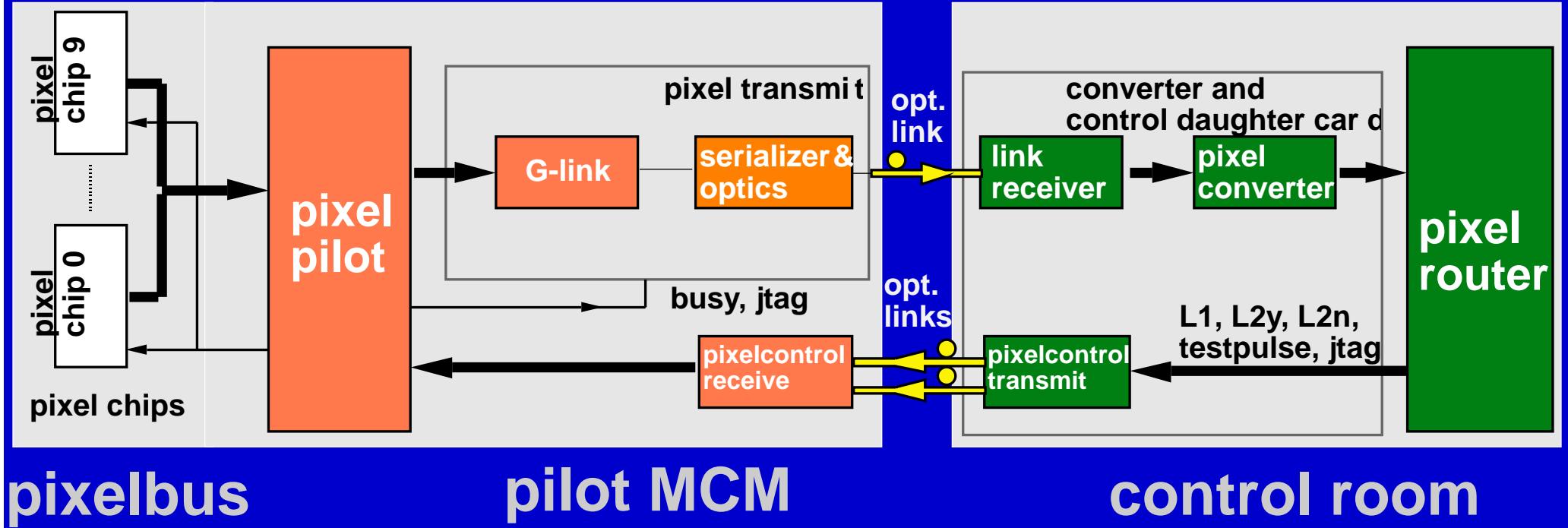


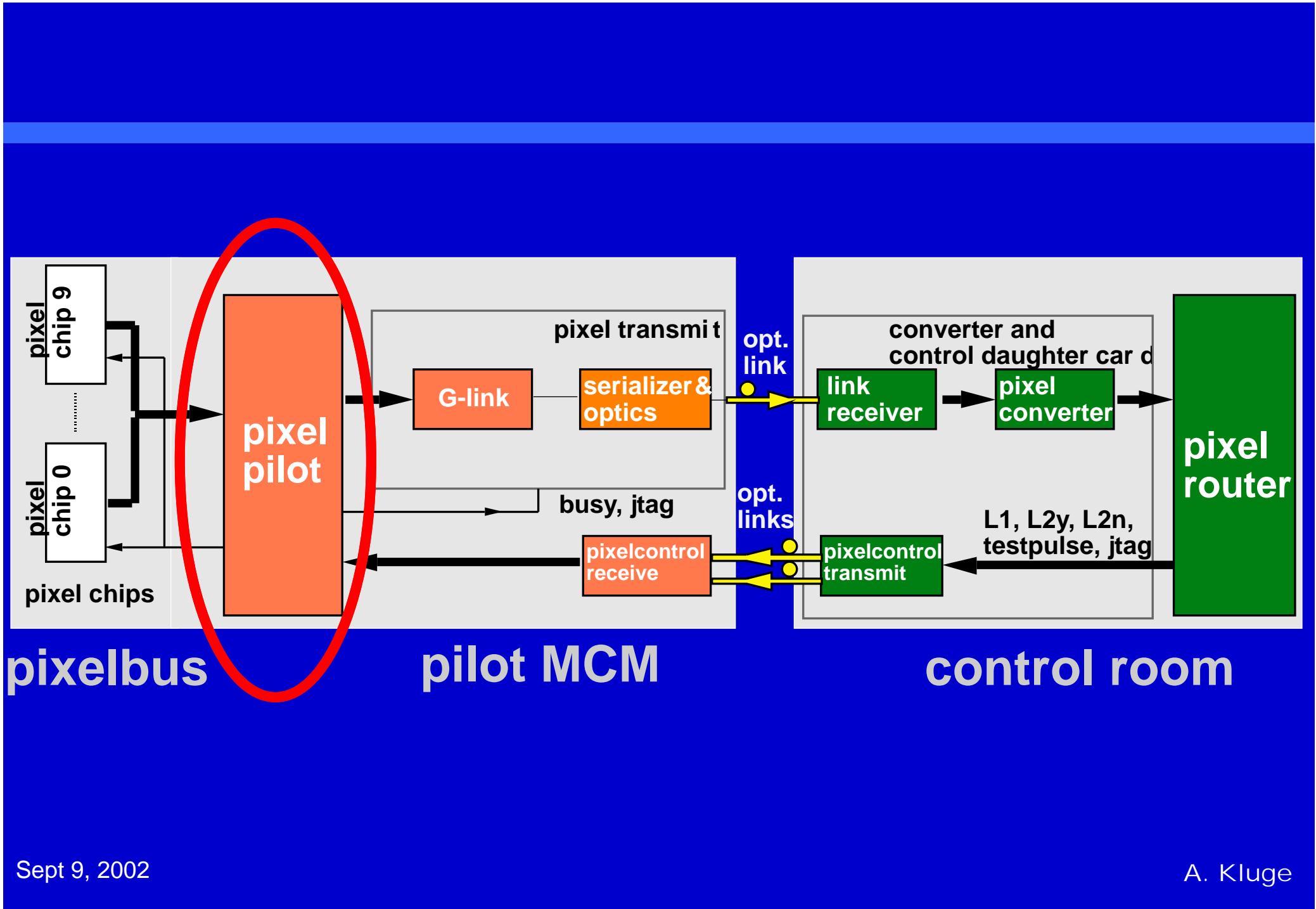
# OPS Tester

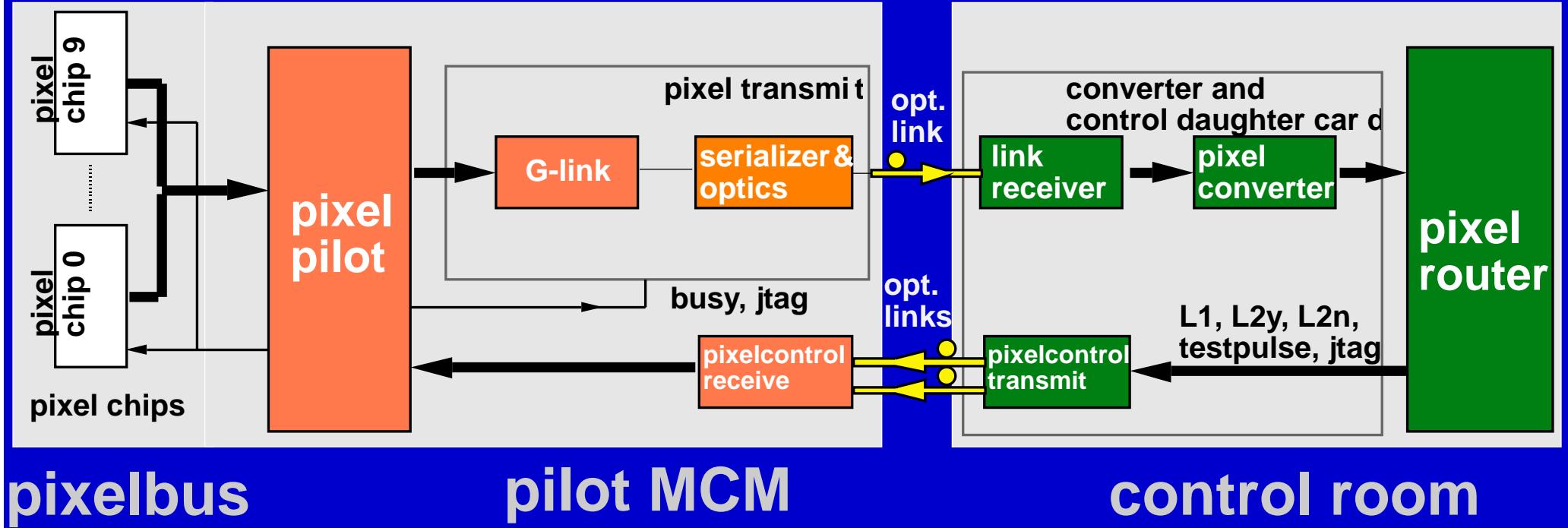


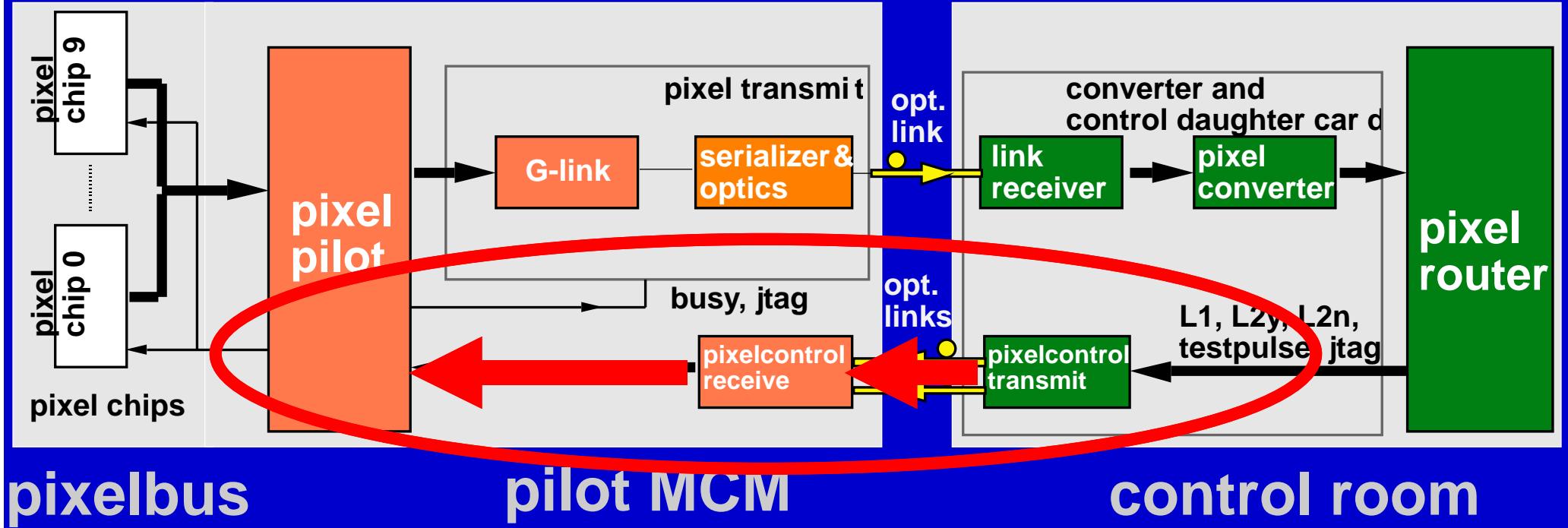
Sept 9, 2002

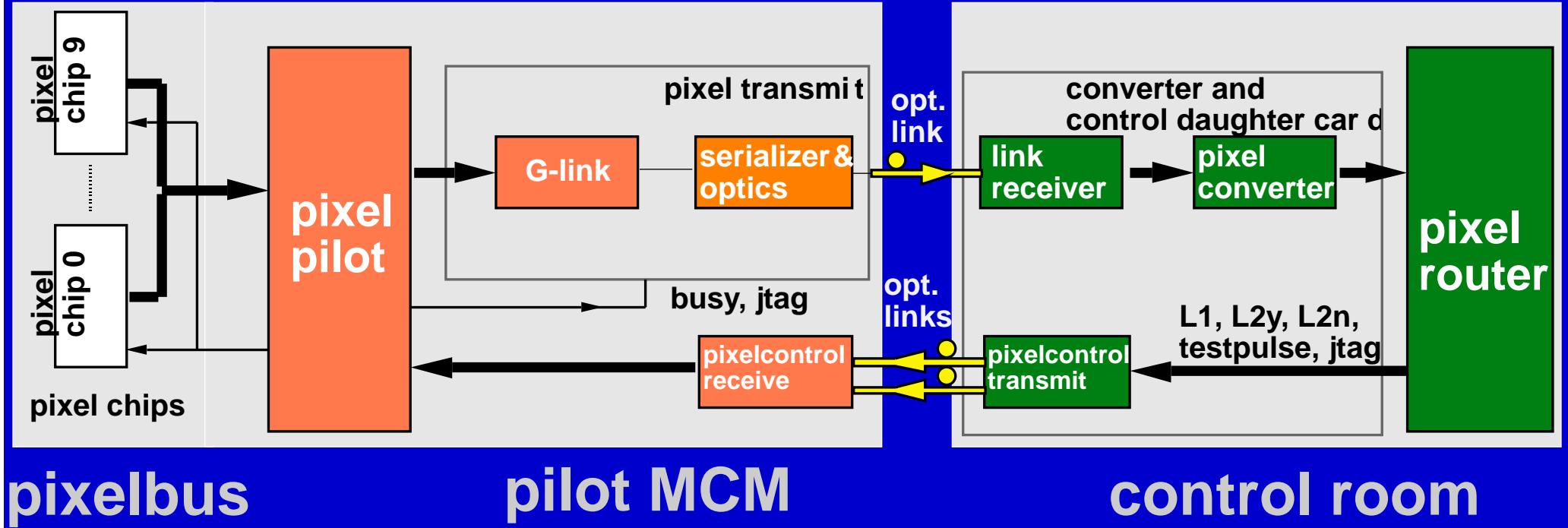
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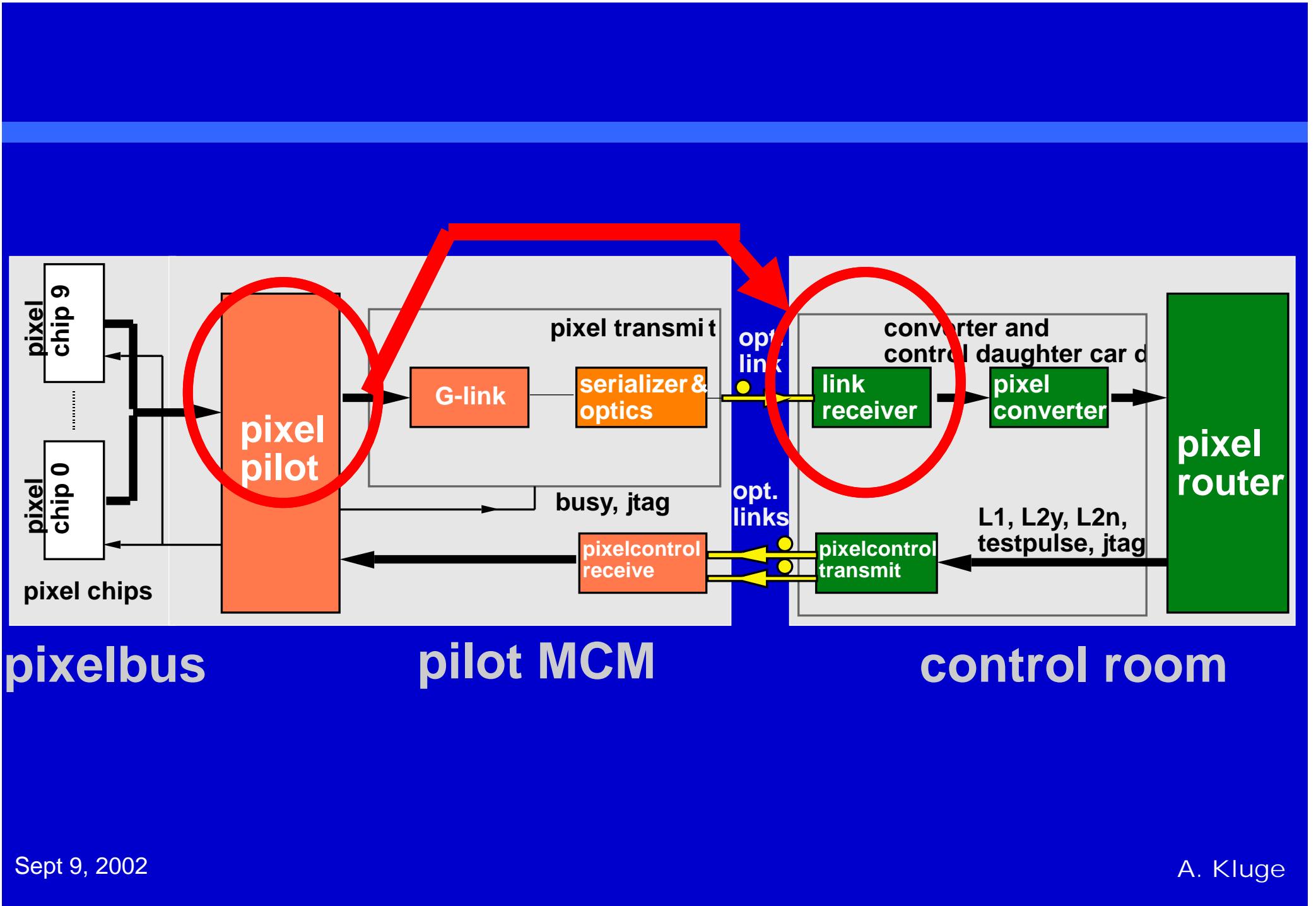


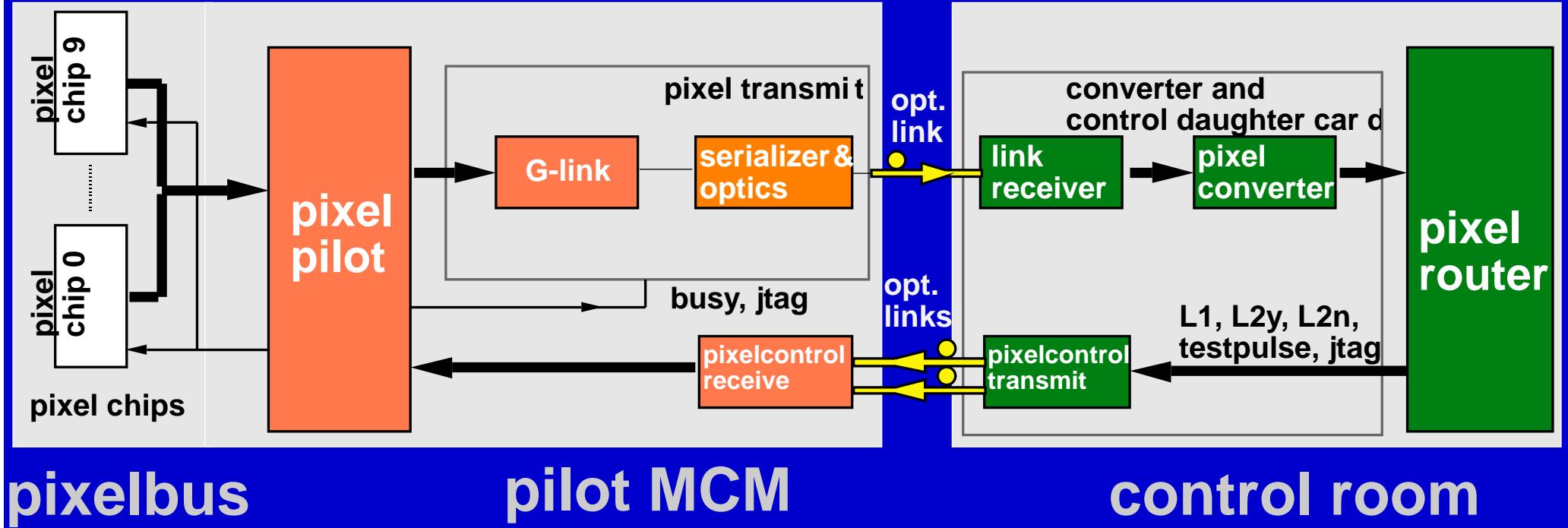


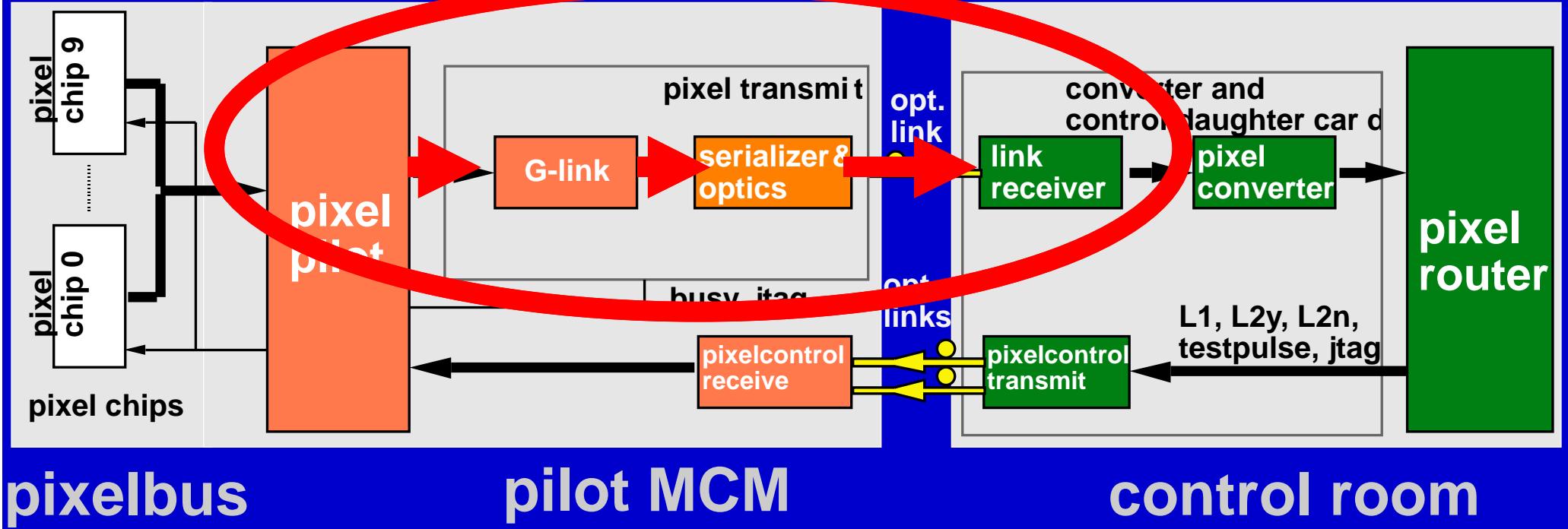


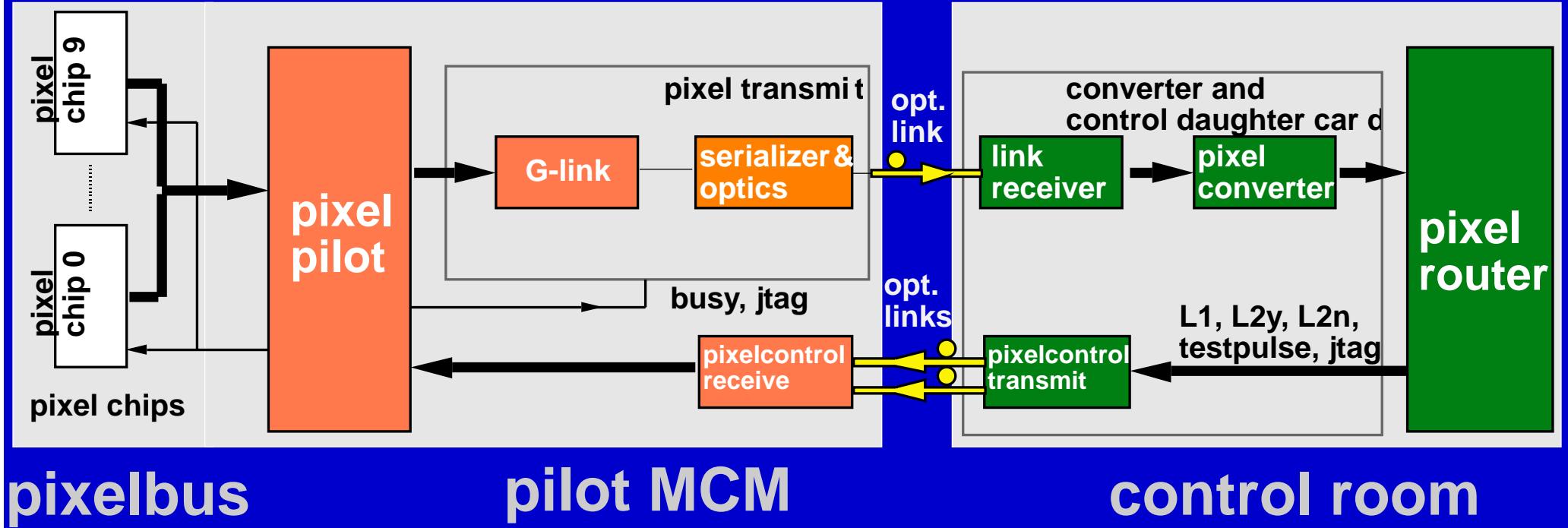


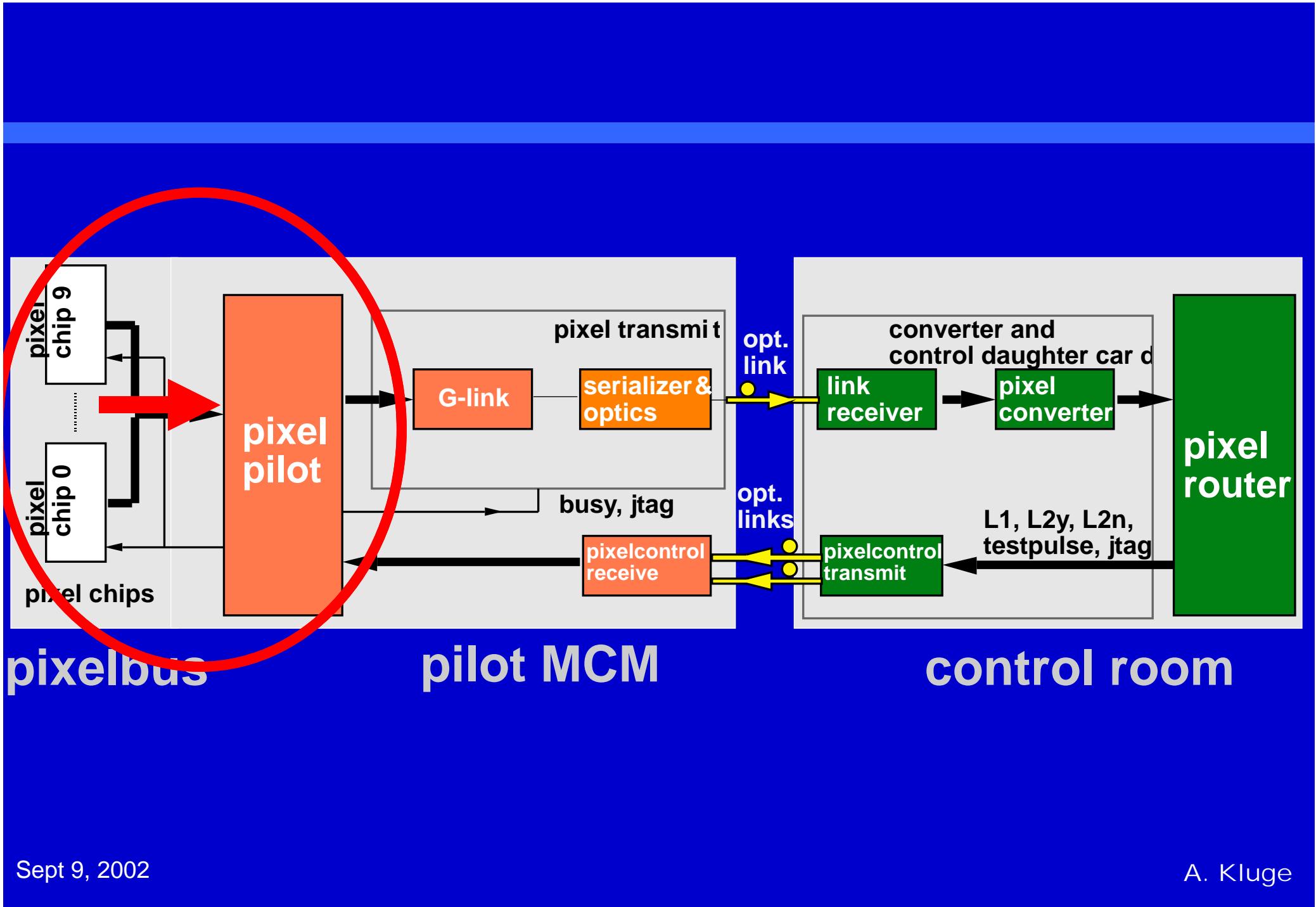


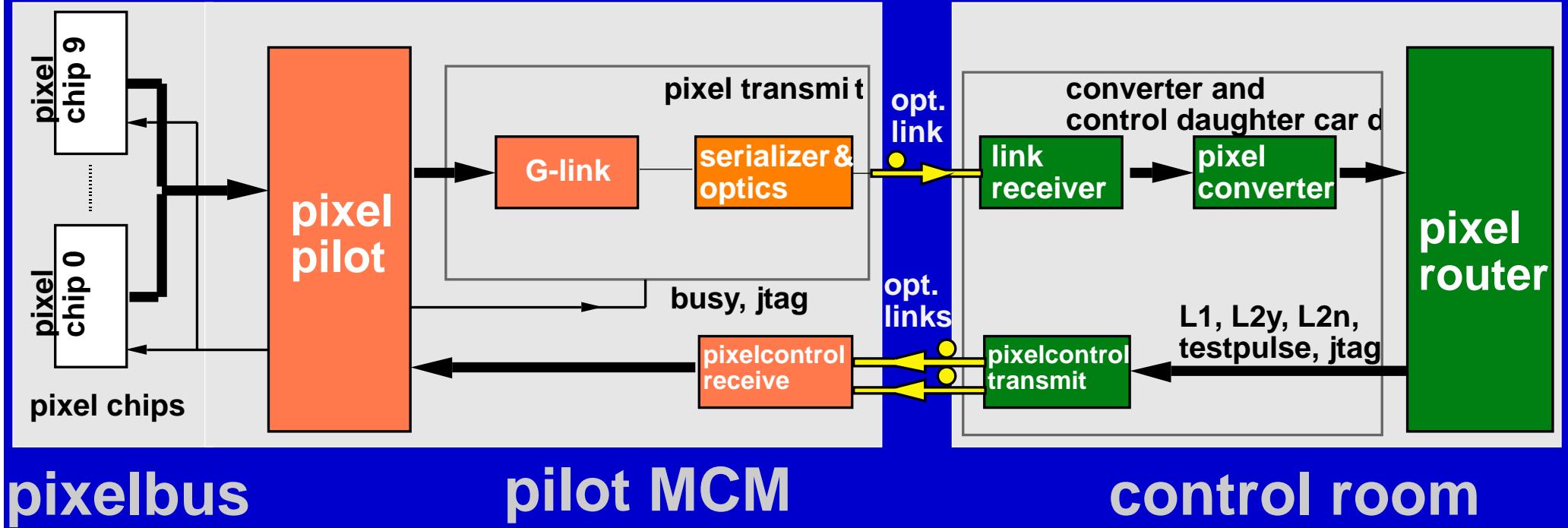












# **Physical implementation**

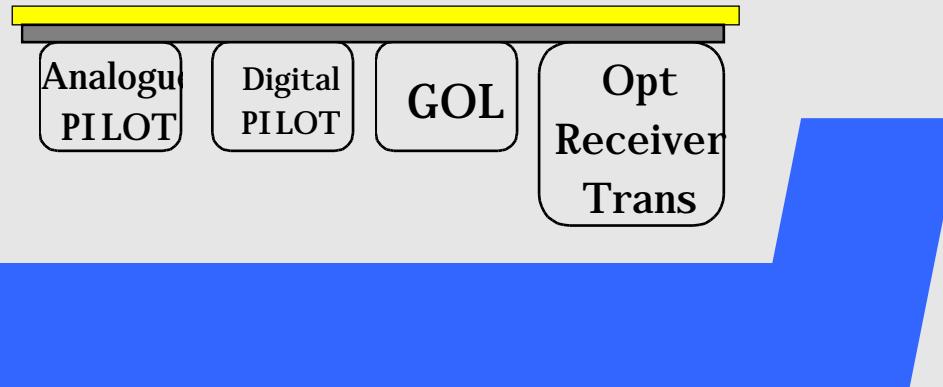
# Pixel carrier & extender (side)



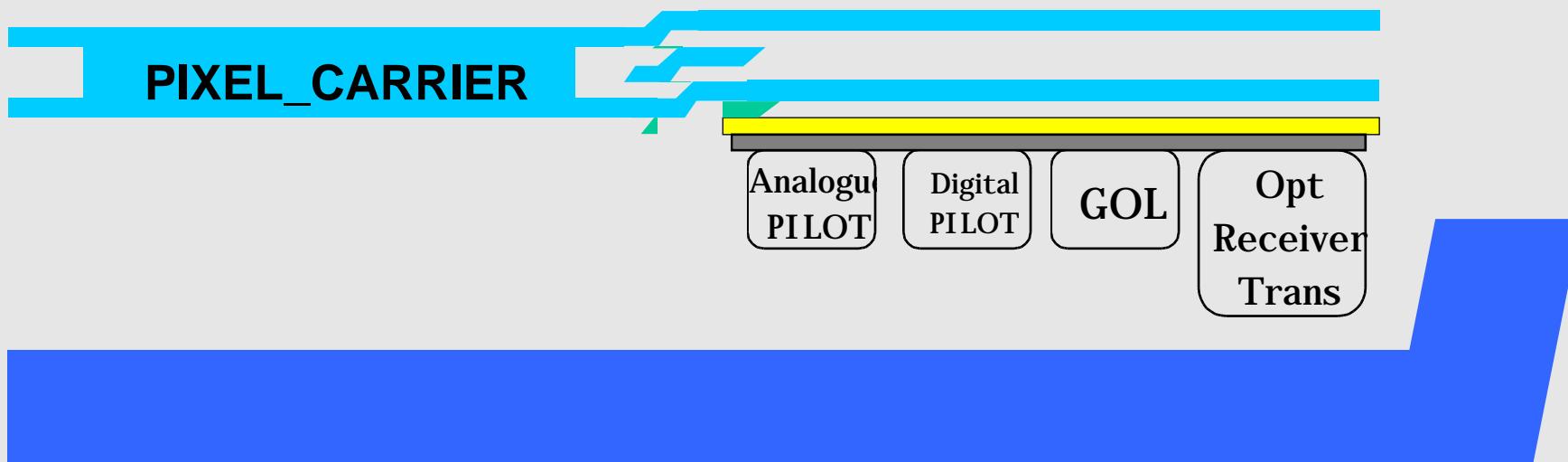
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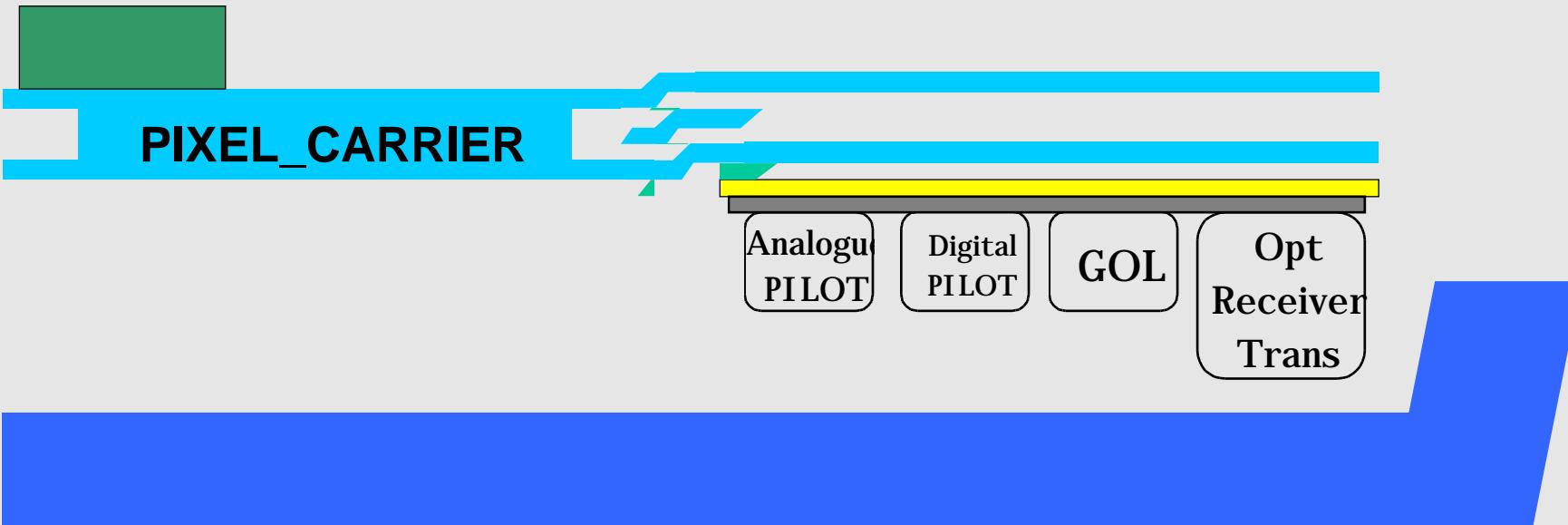


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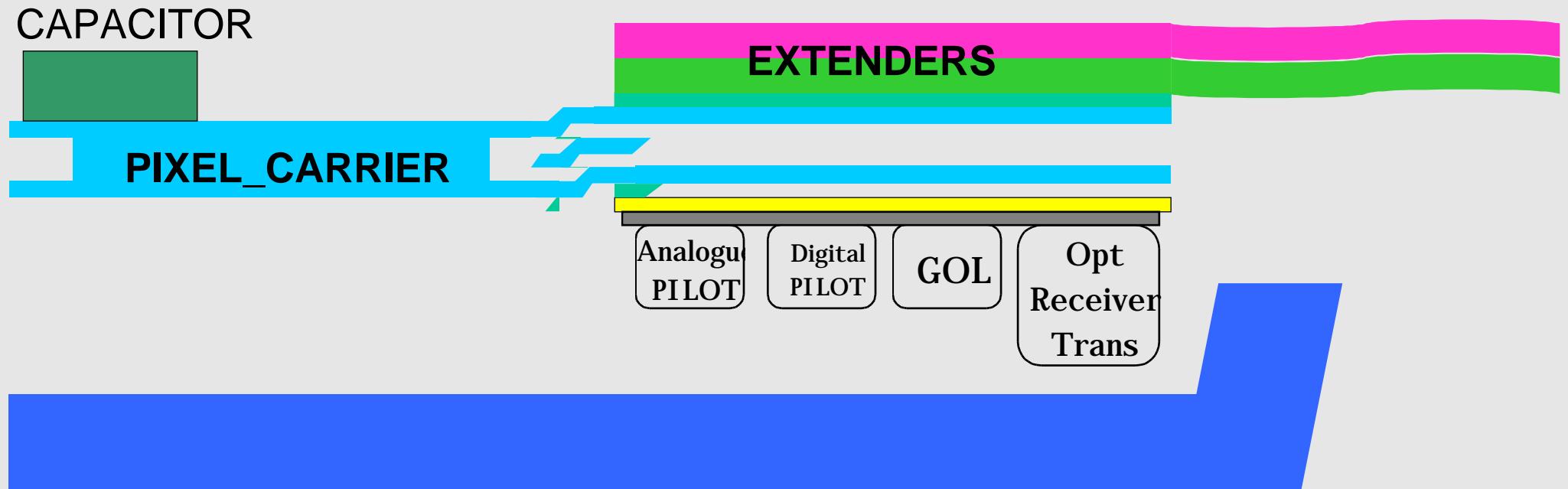


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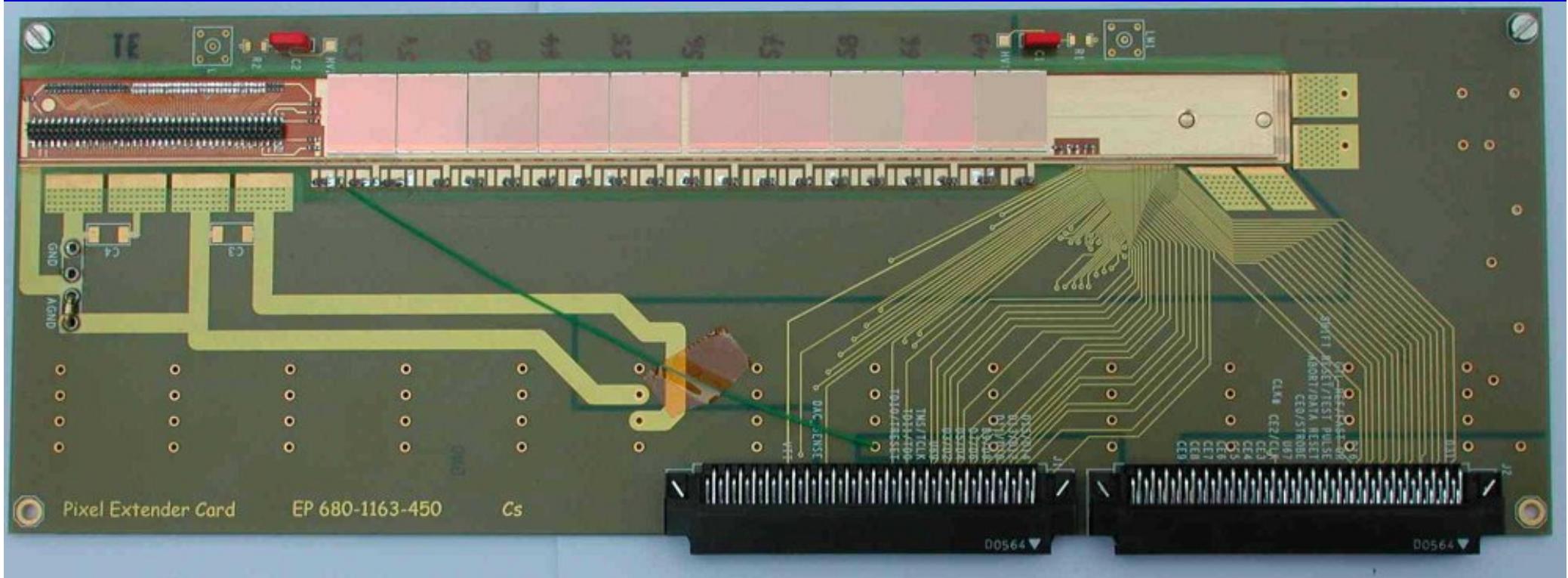
CAPACITOR



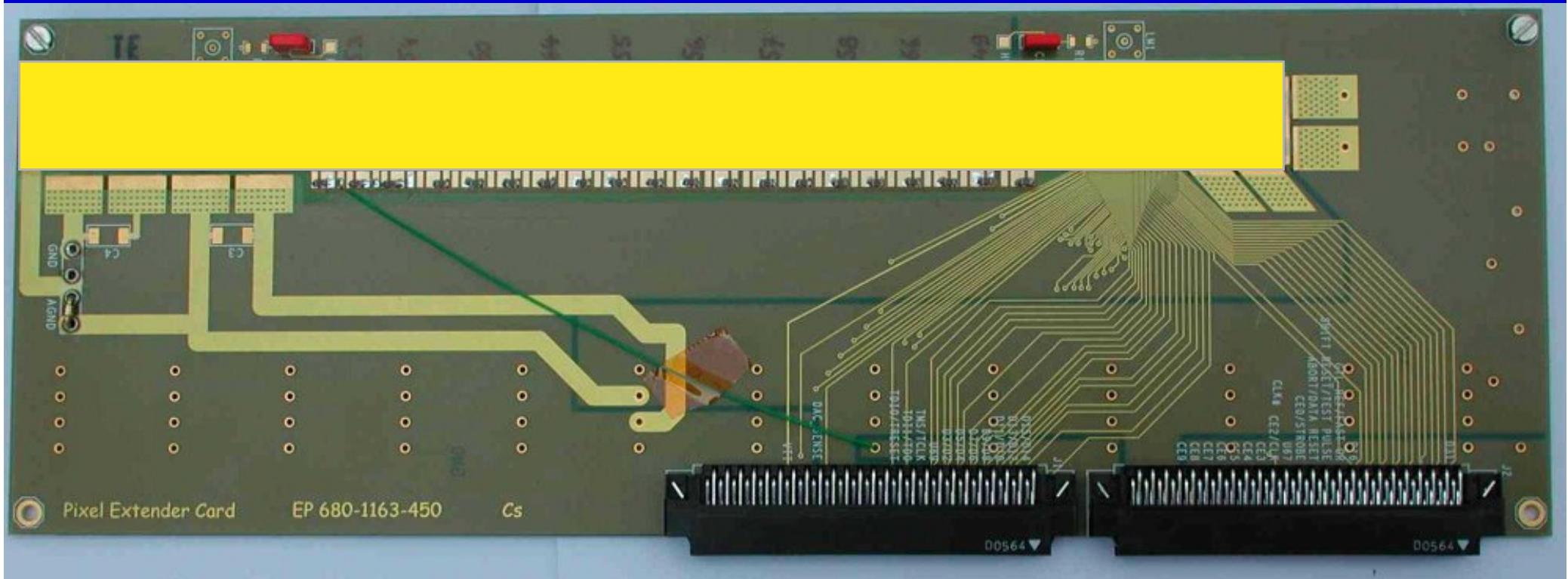
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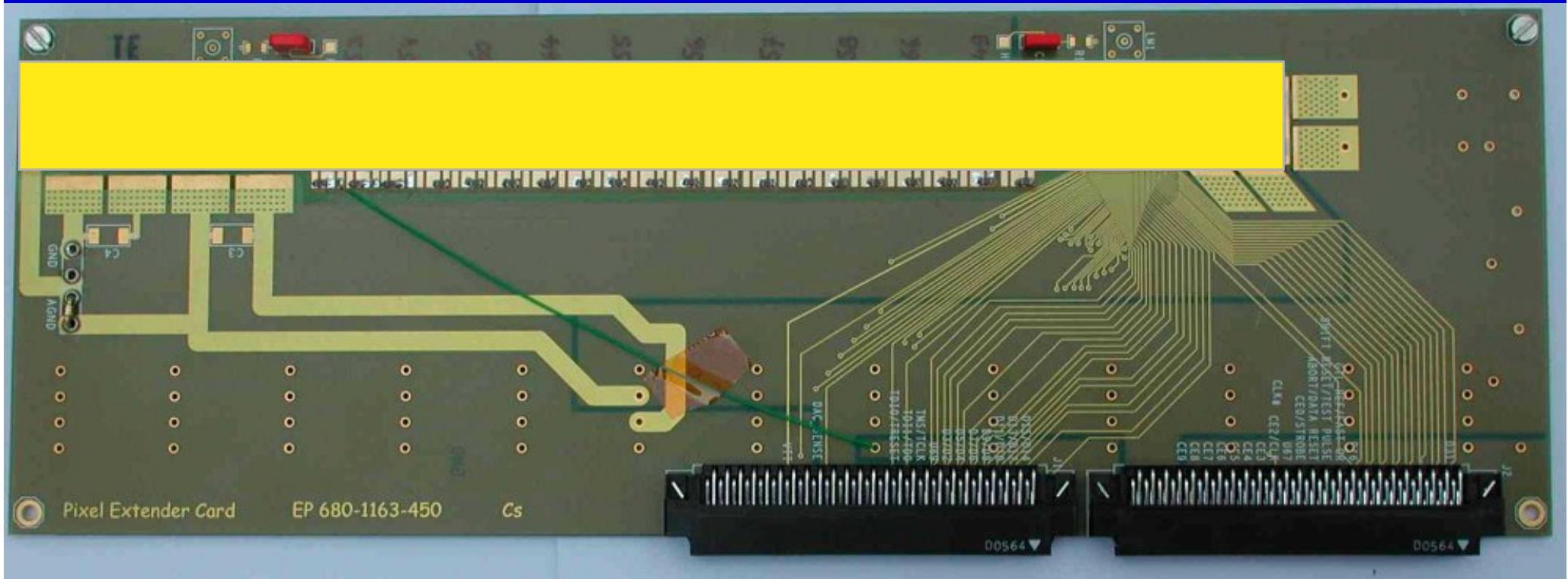
# 10 chips on a carrier



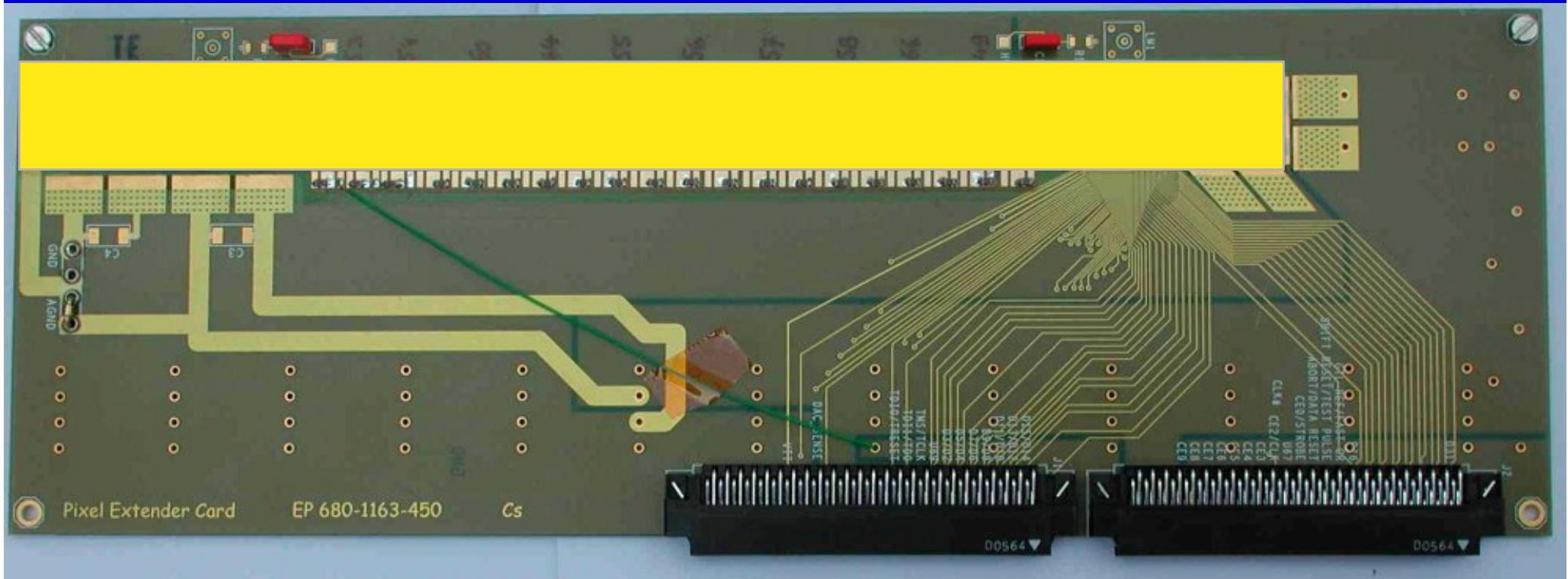
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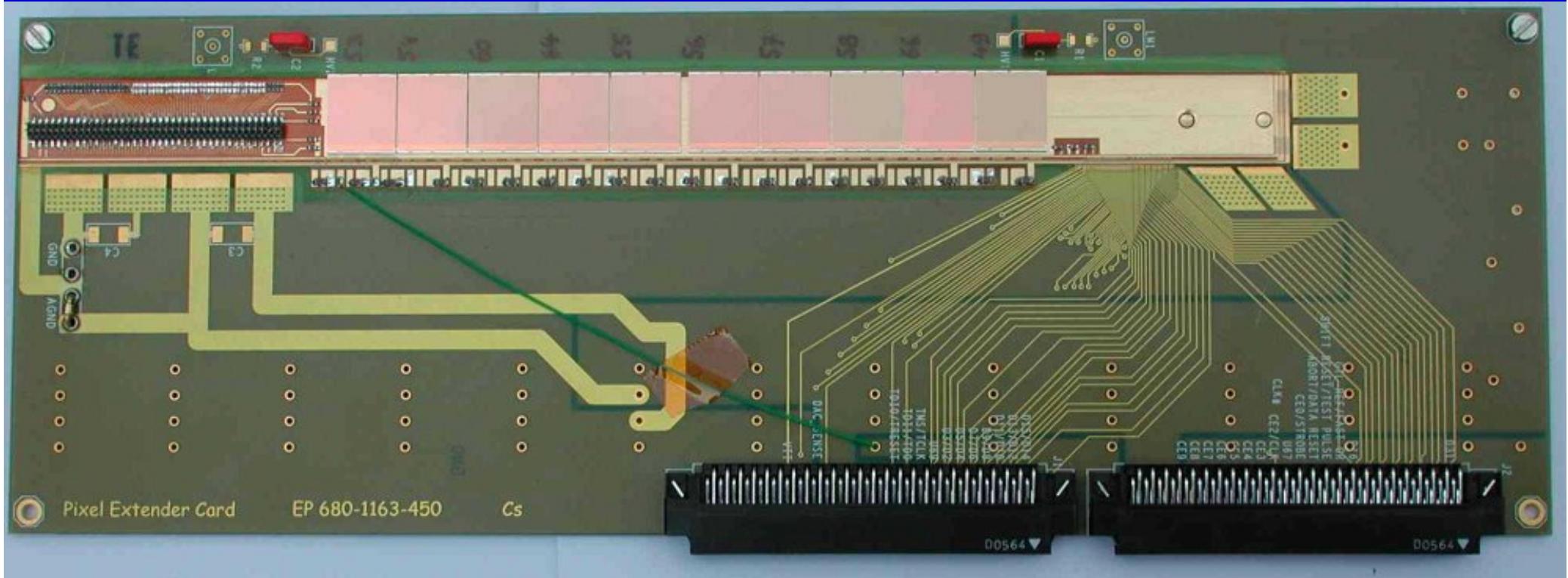
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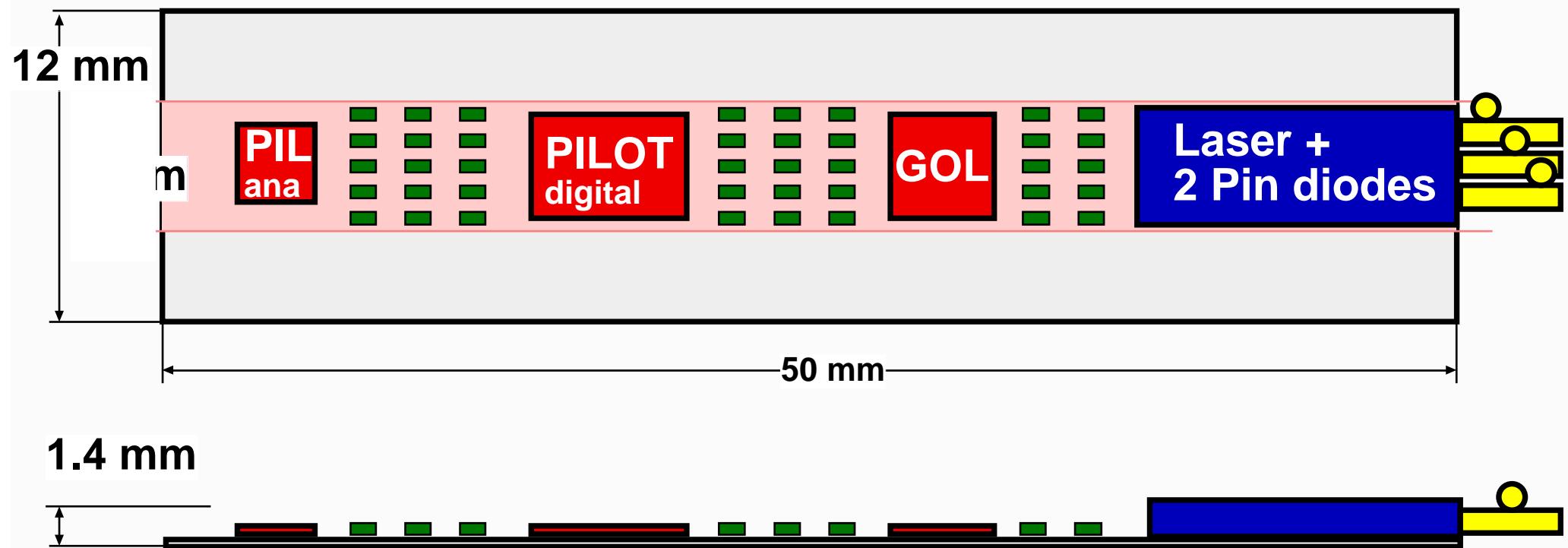
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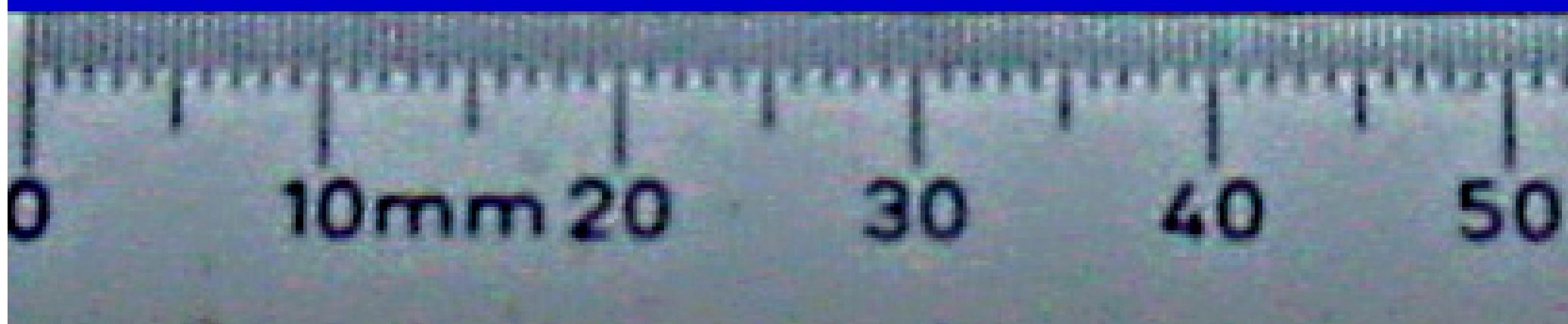
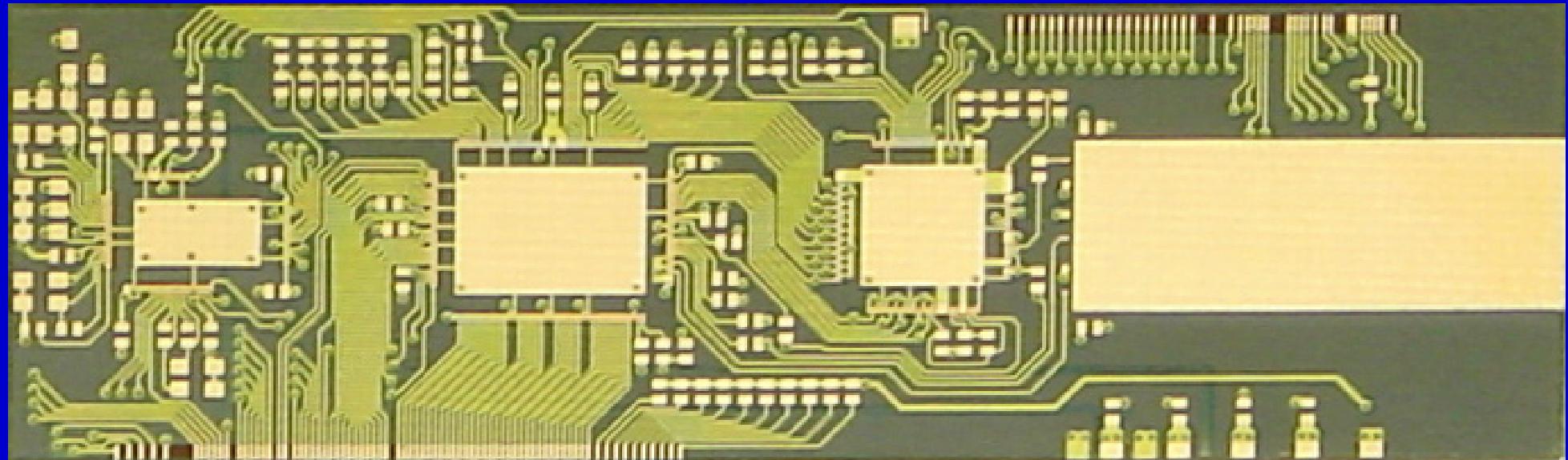
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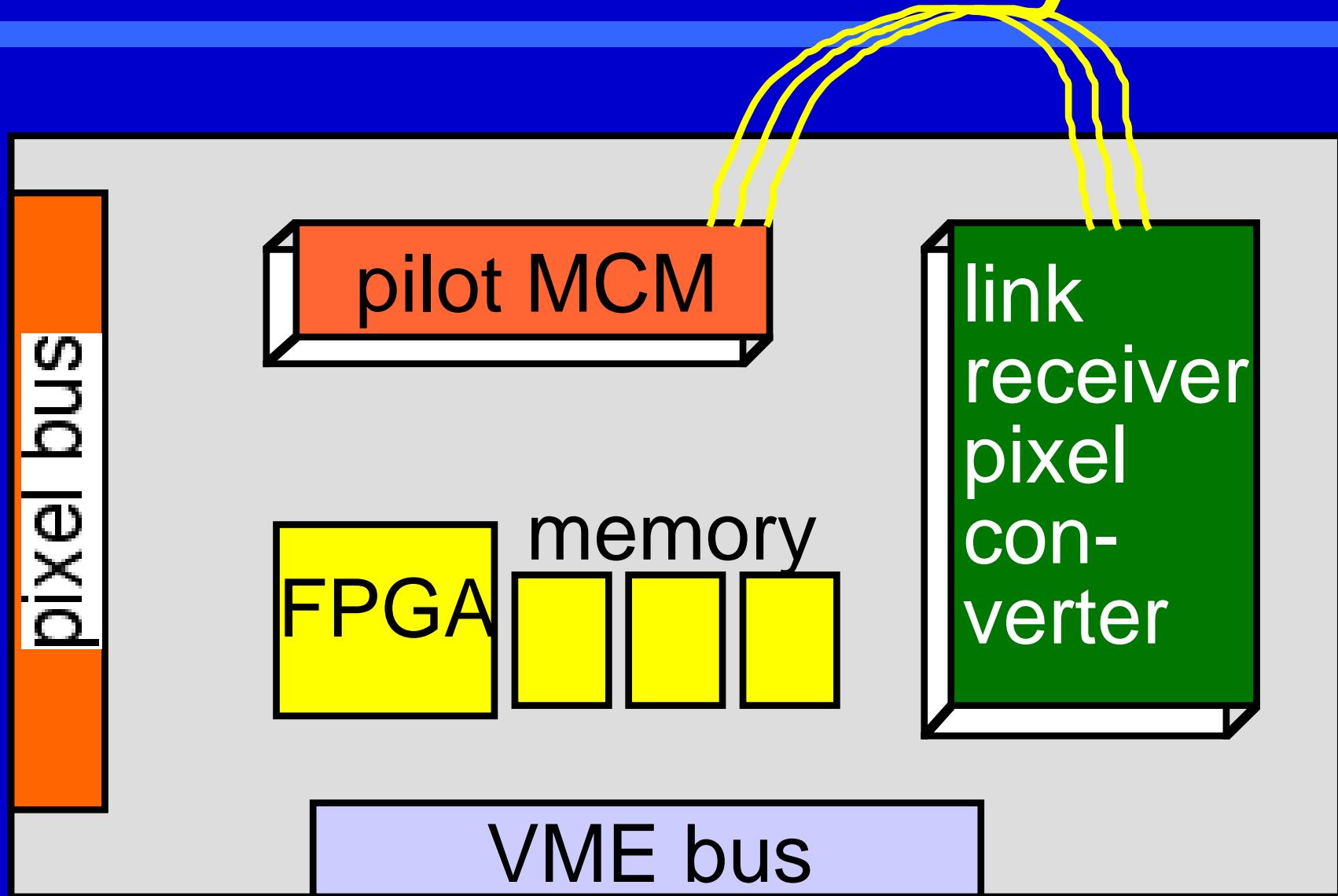
# Pilot MCM



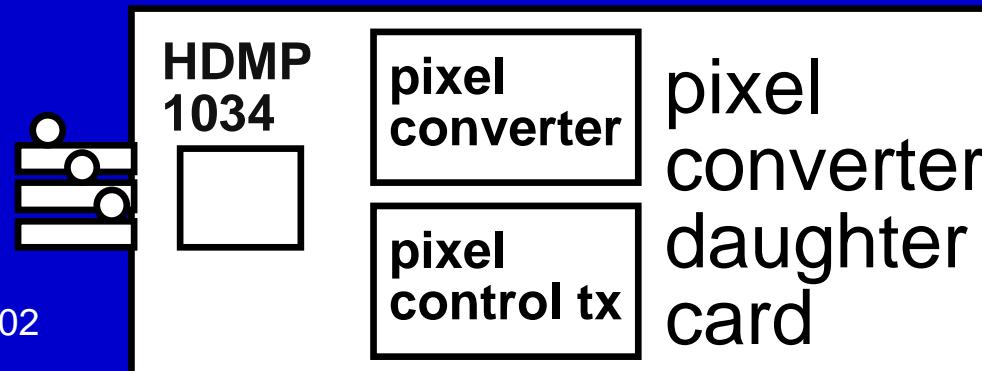
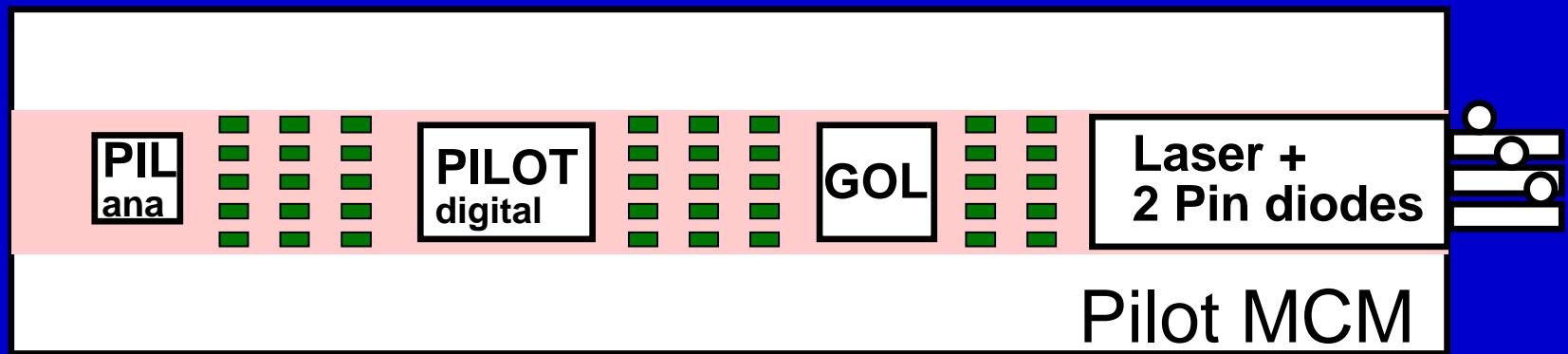
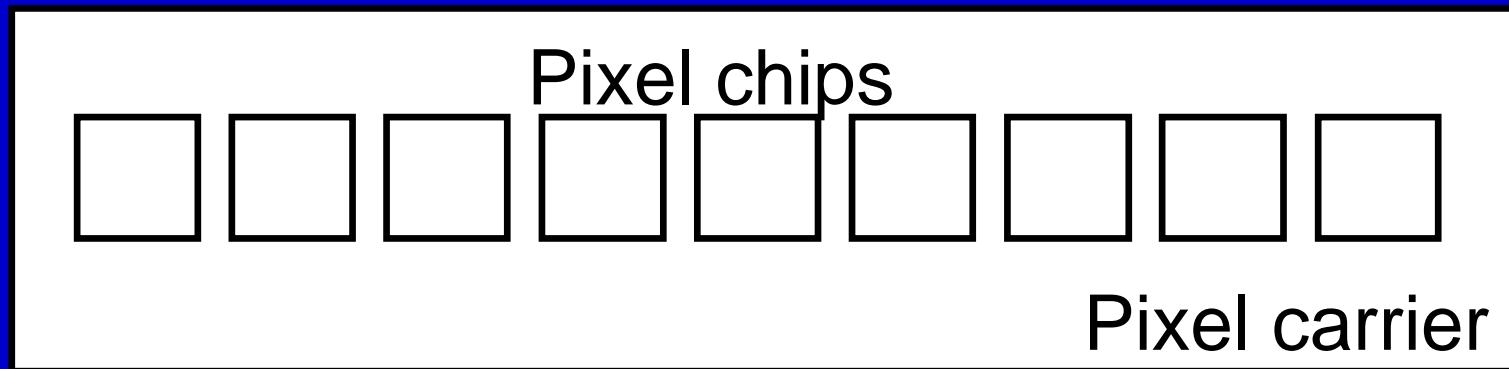
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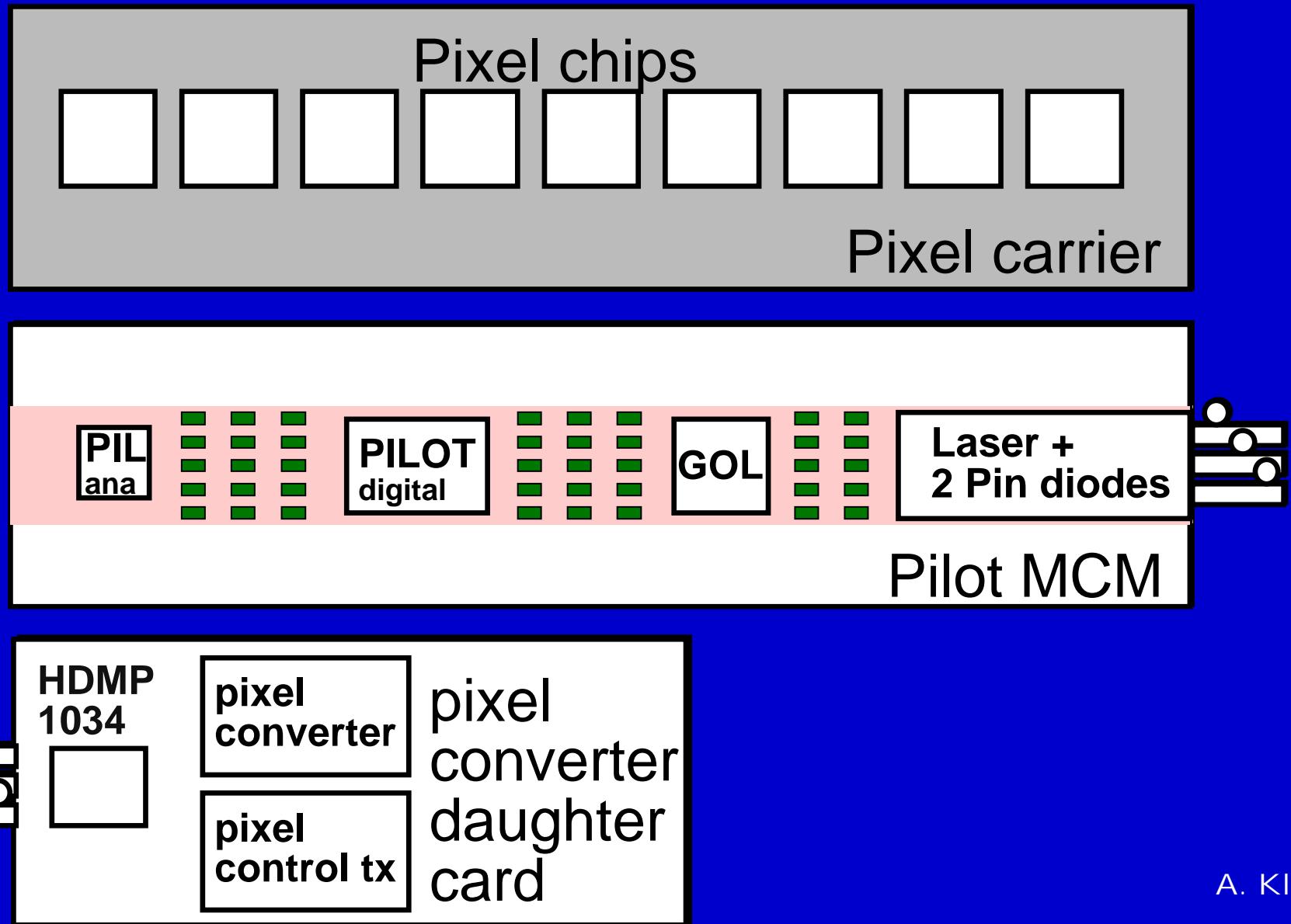
# Pixel Readout Test System



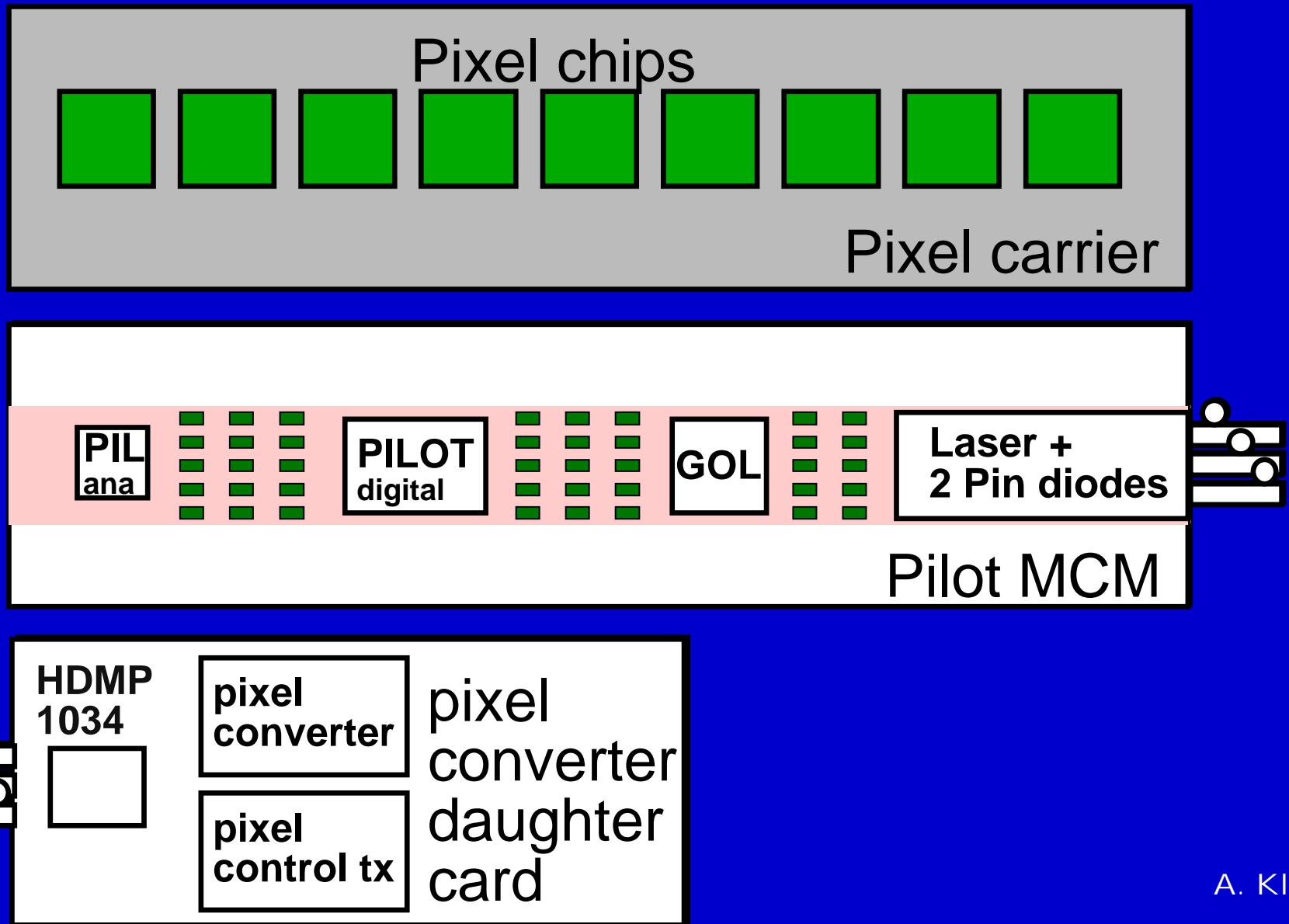
# Component Status



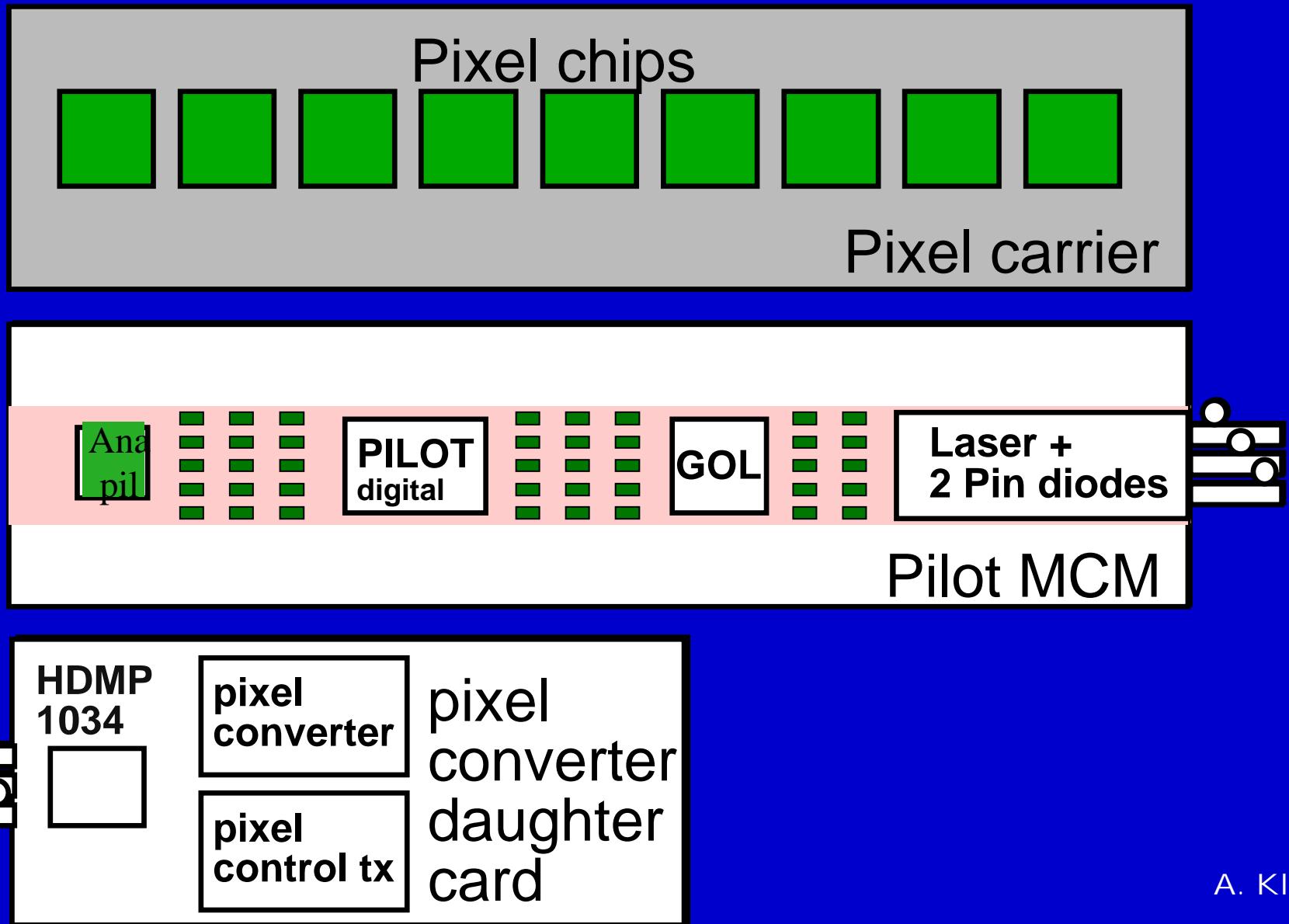
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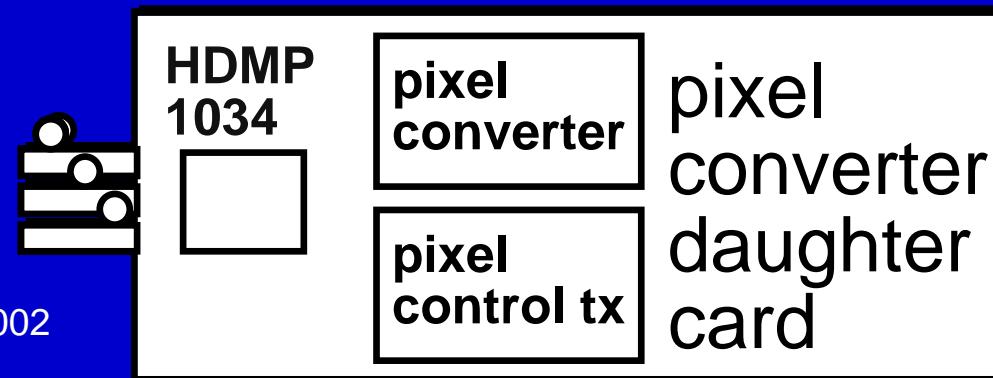
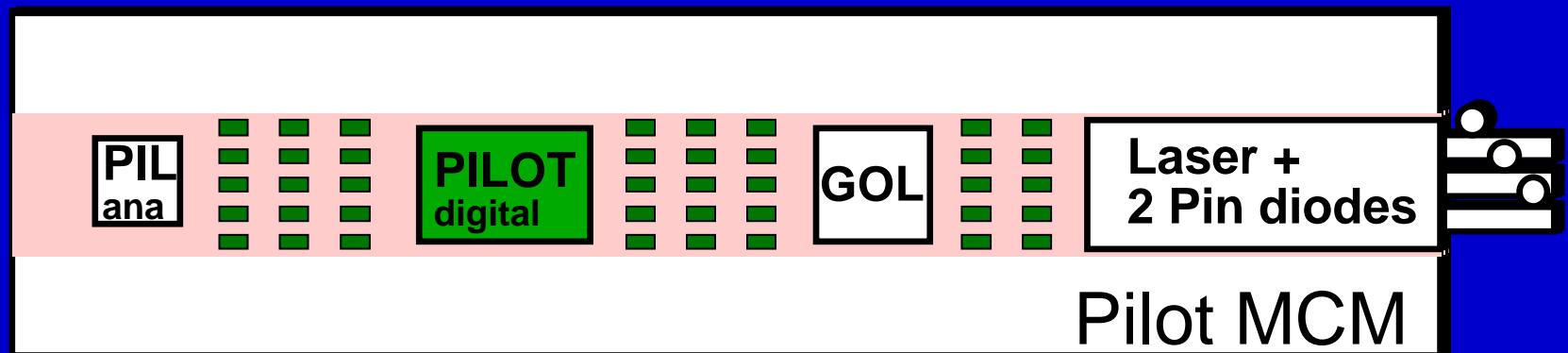
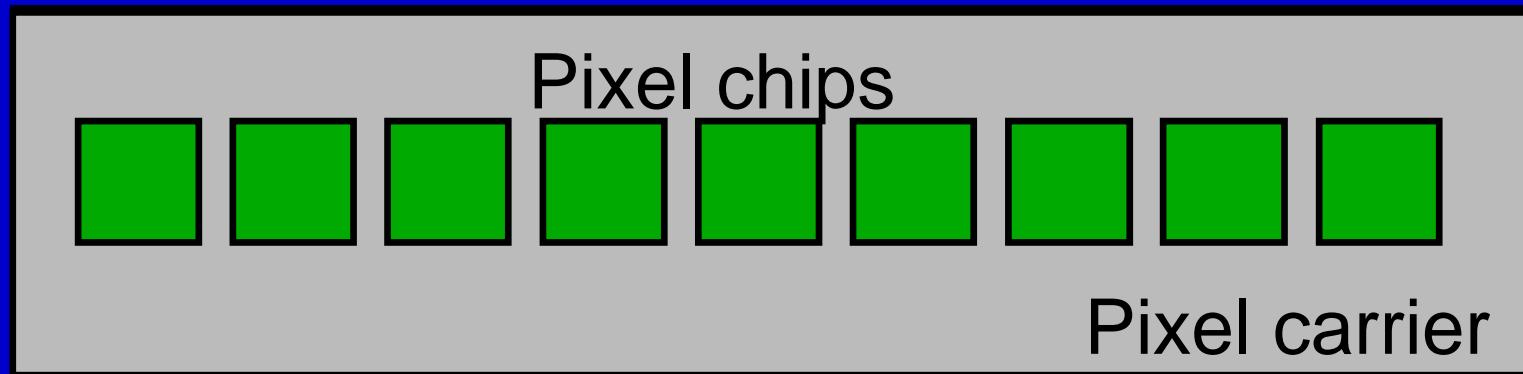
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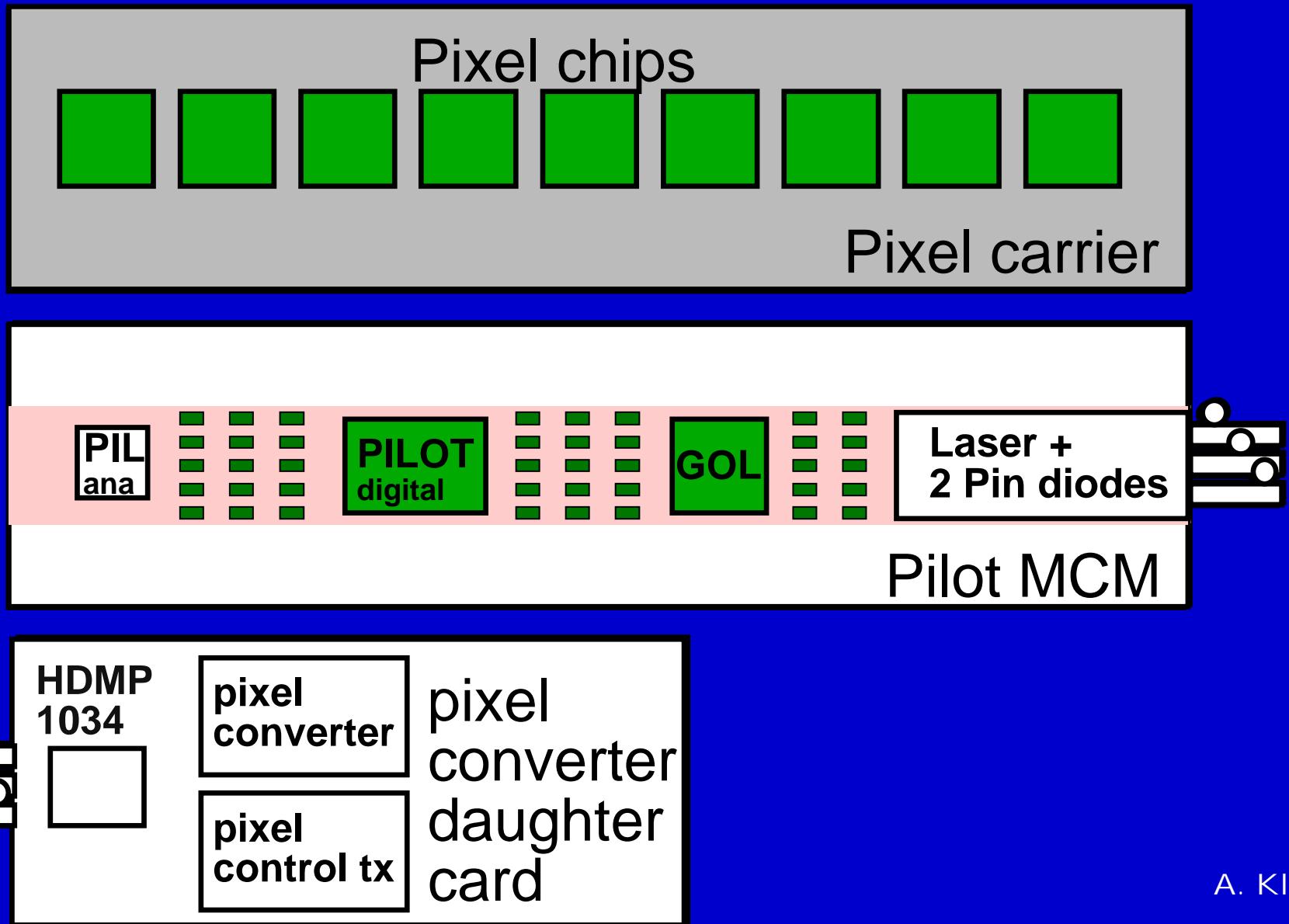
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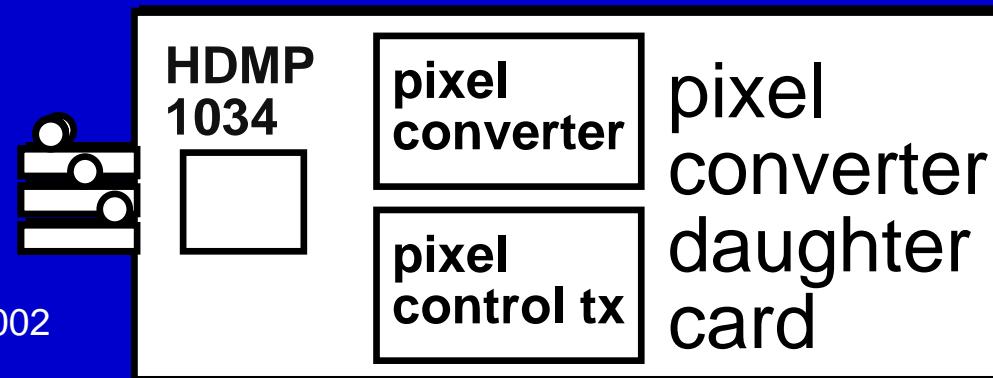
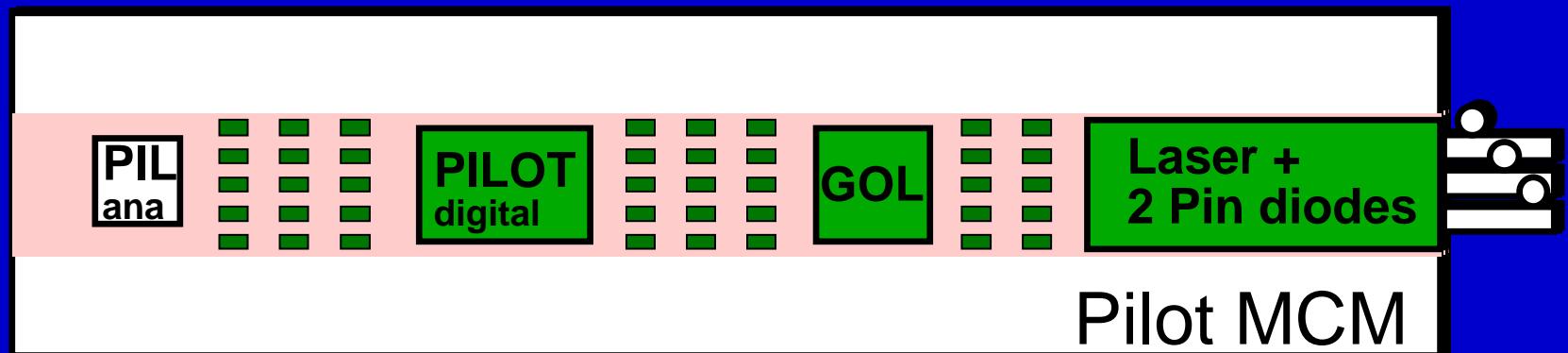
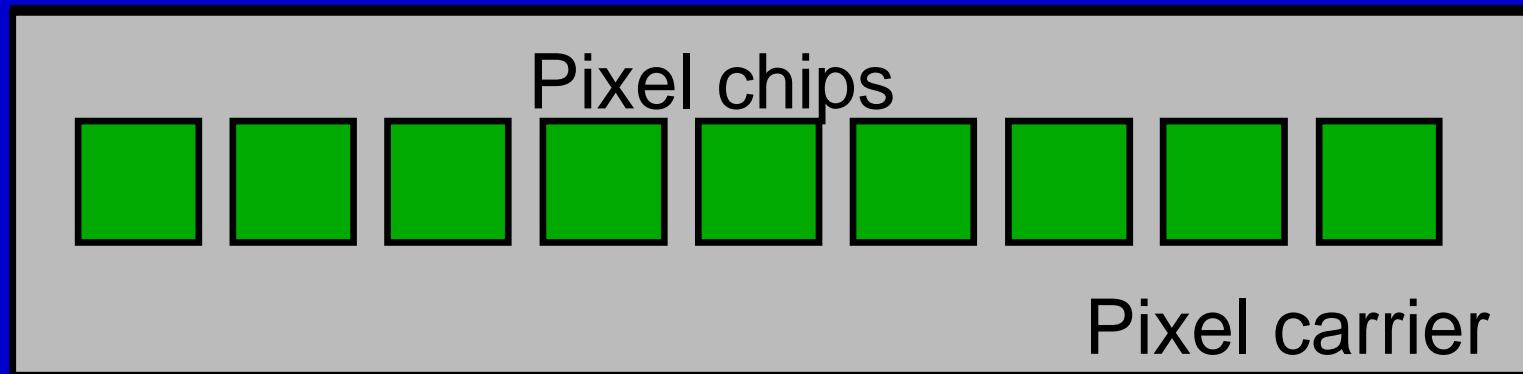
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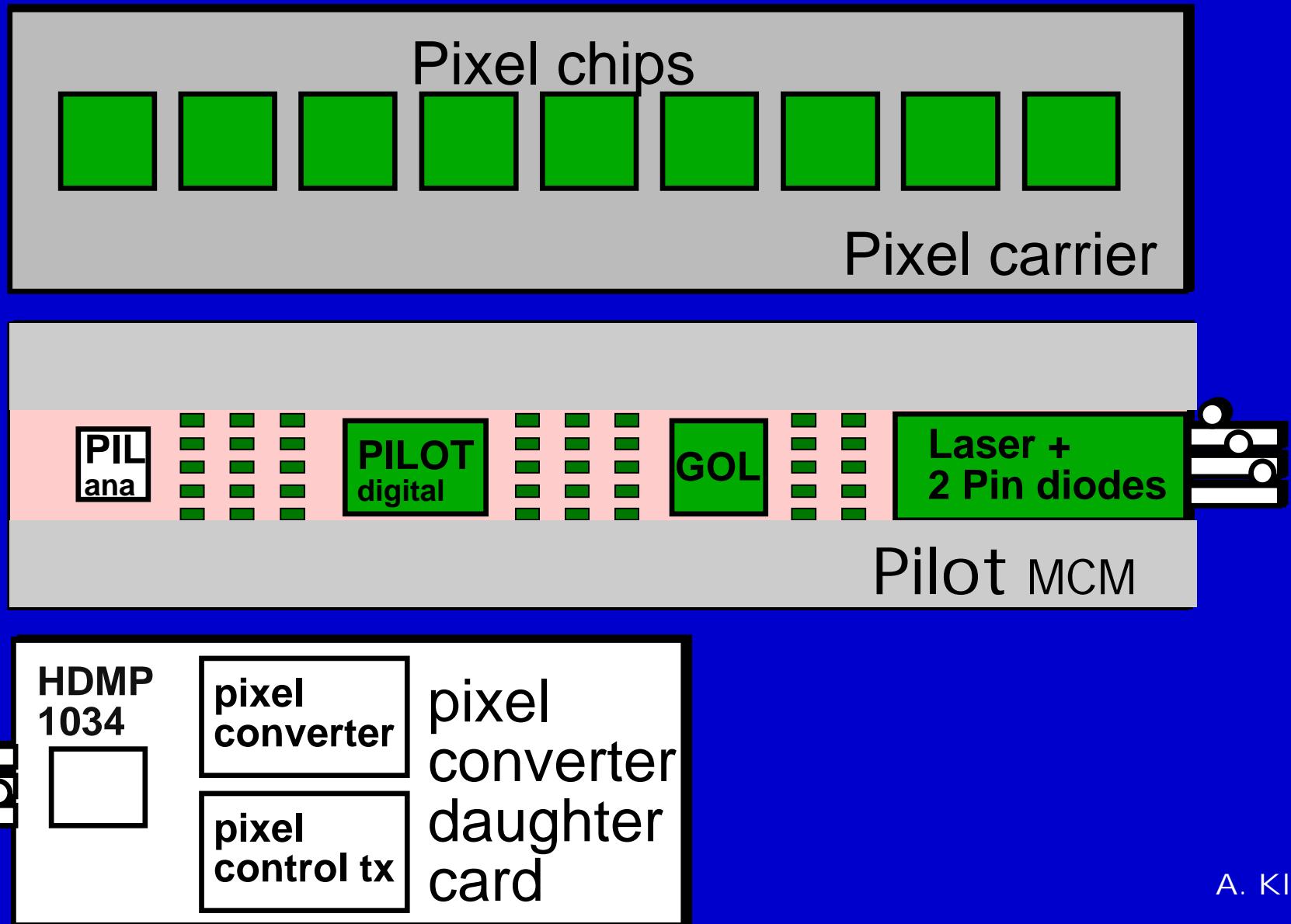
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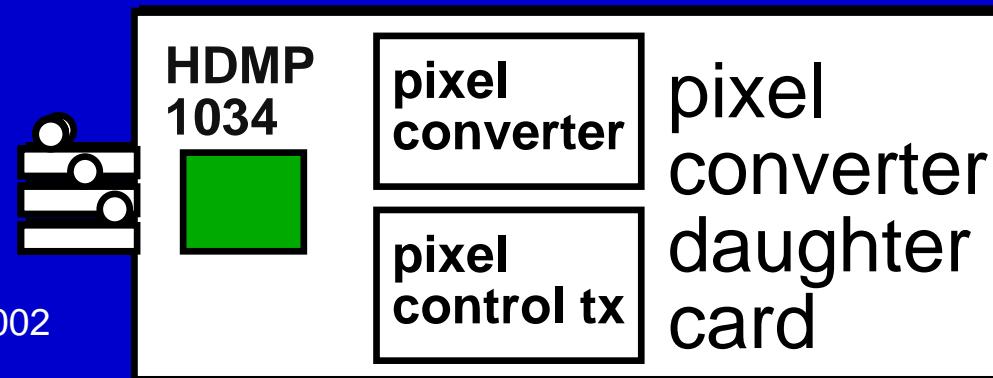
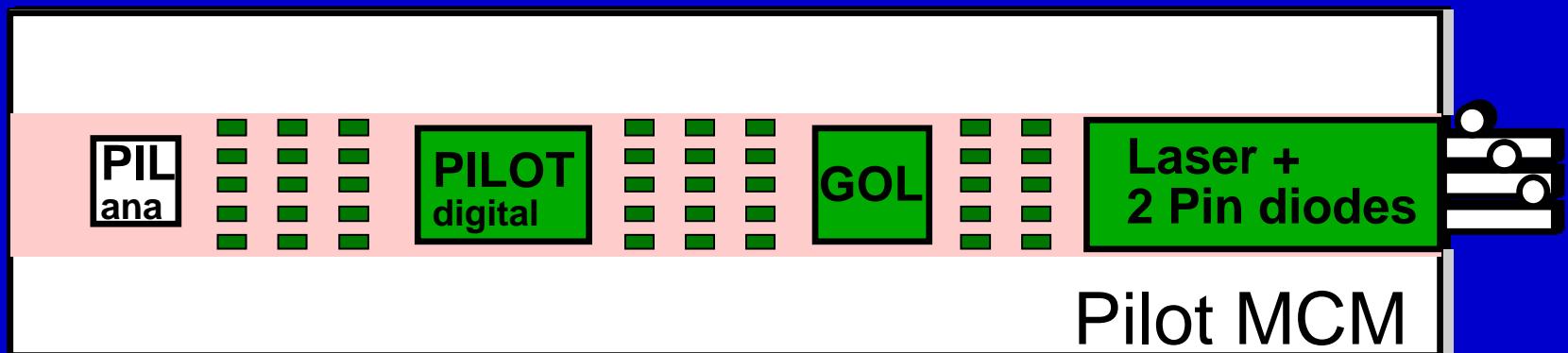
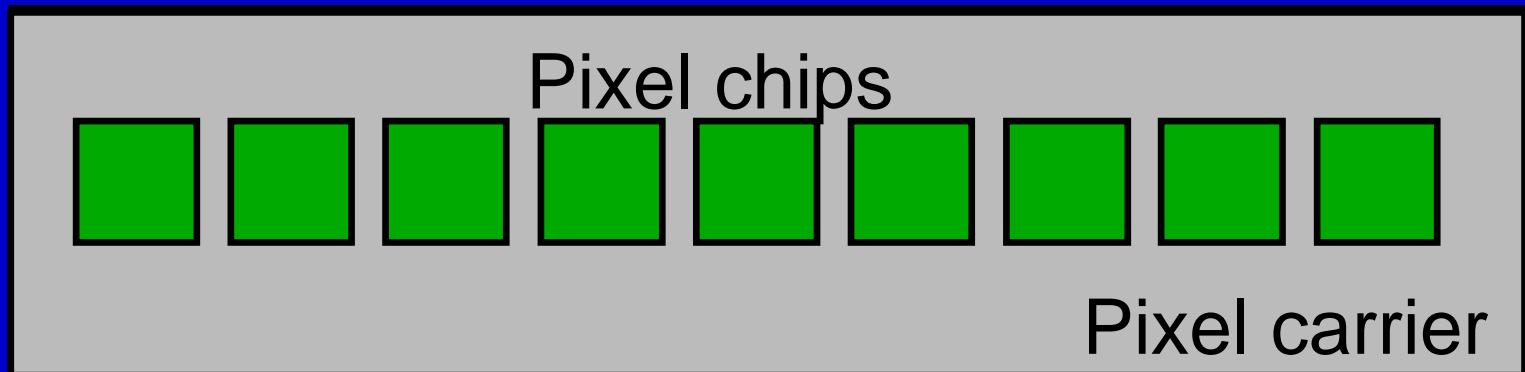
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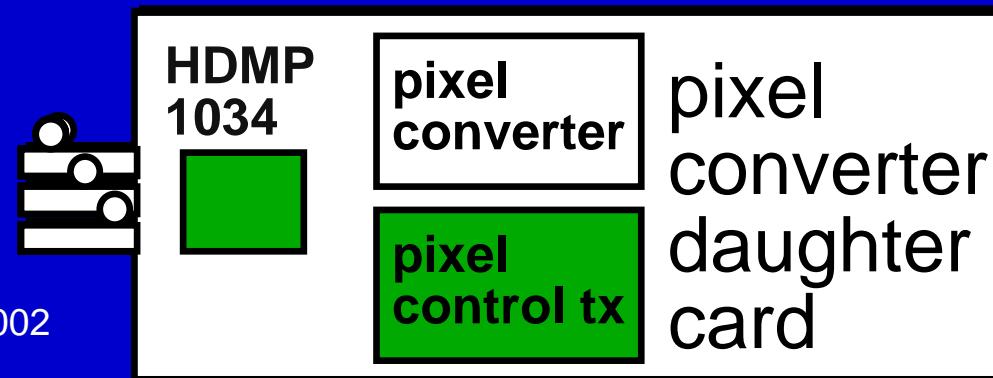
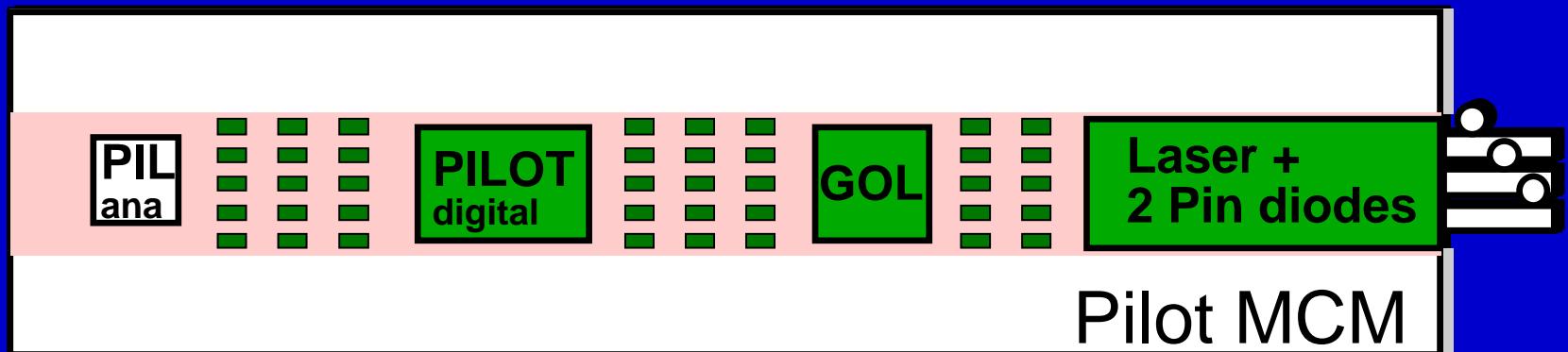
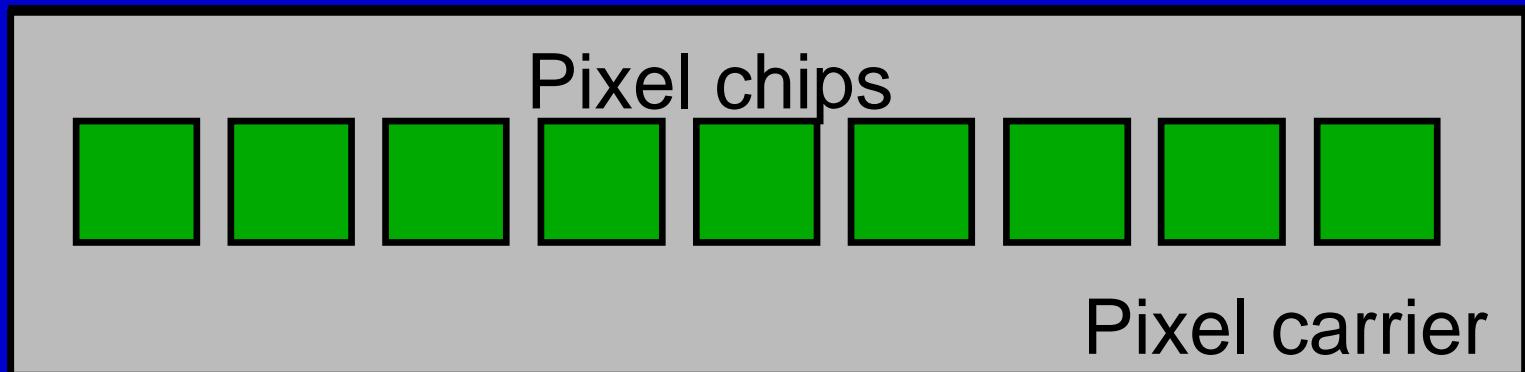
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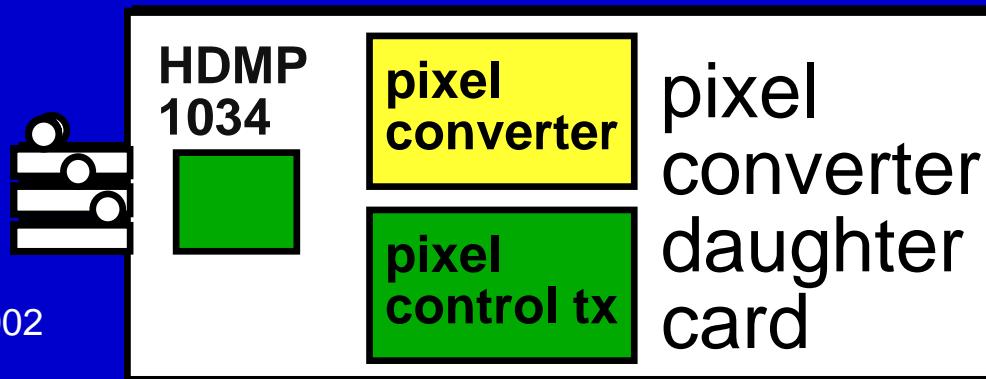
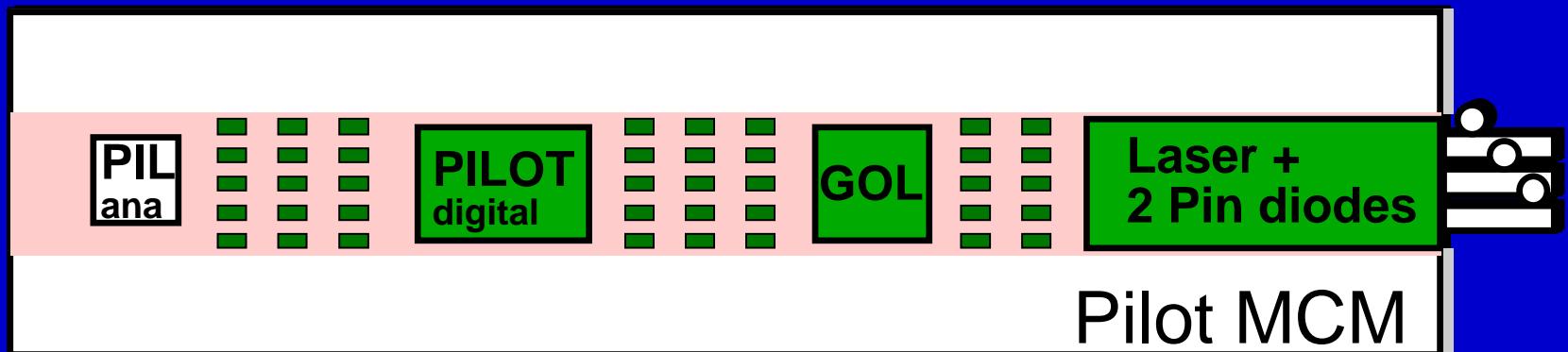
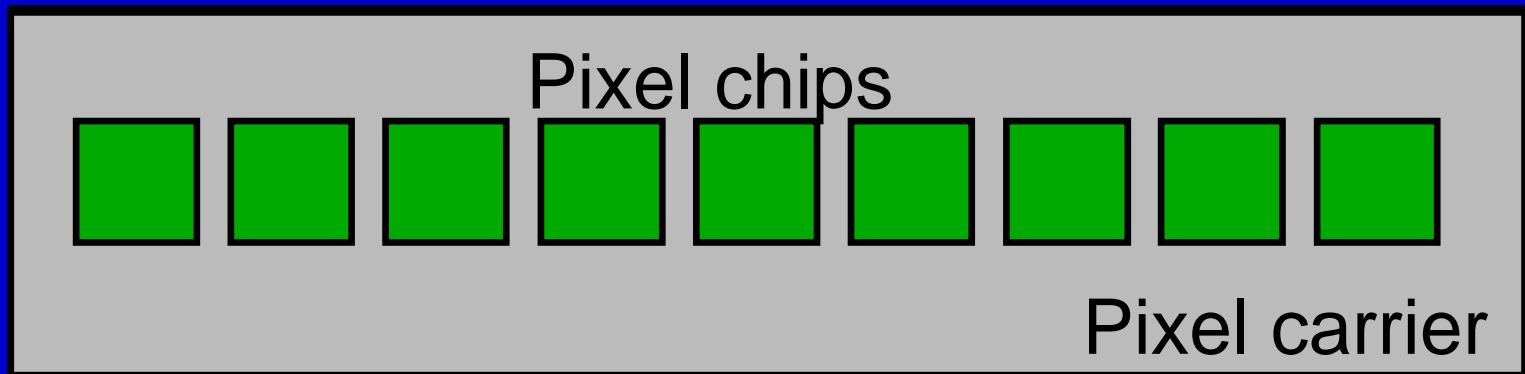
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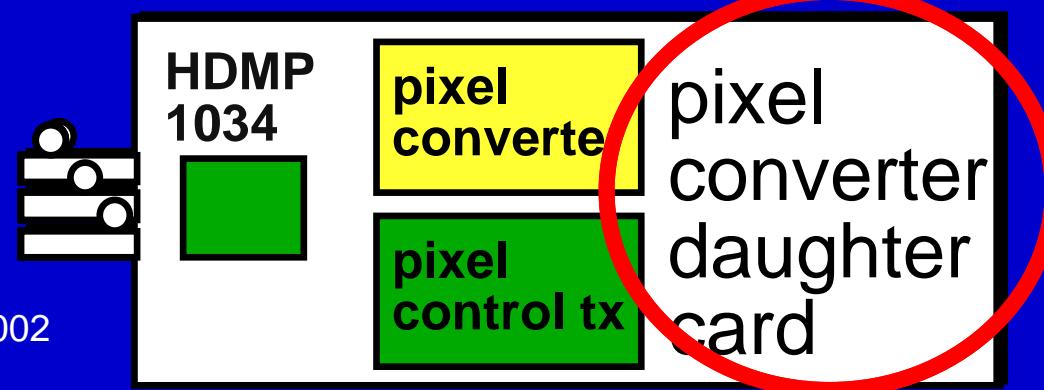
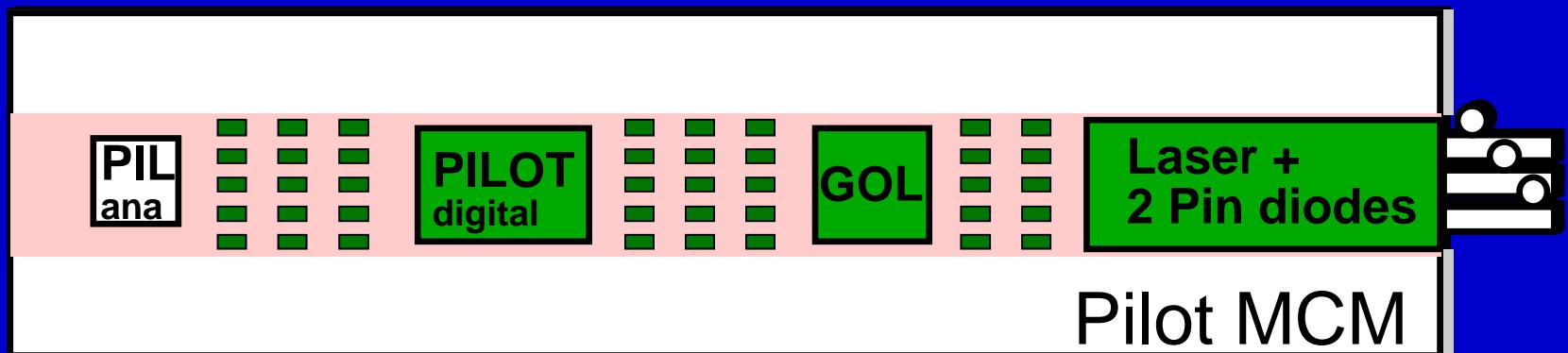
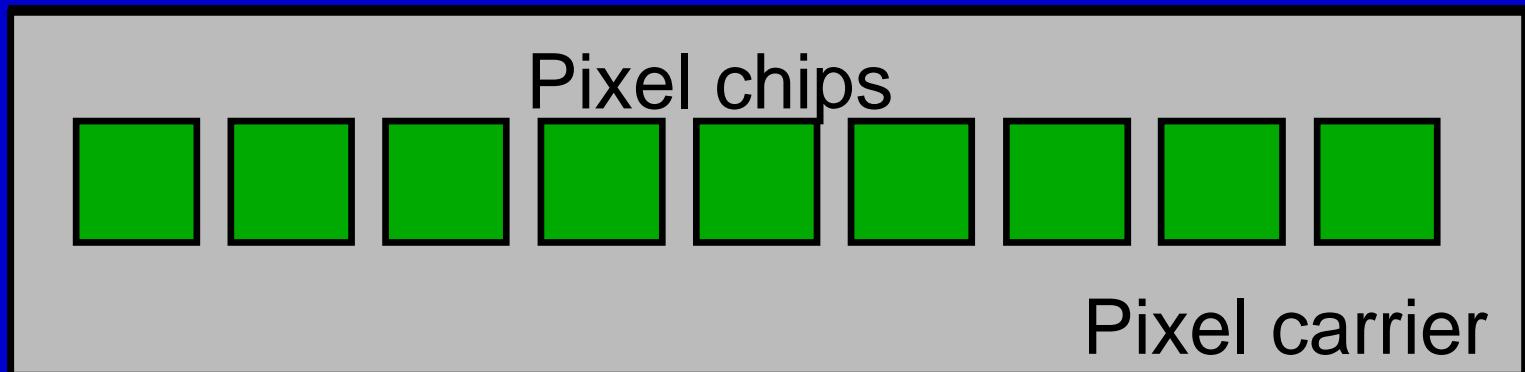
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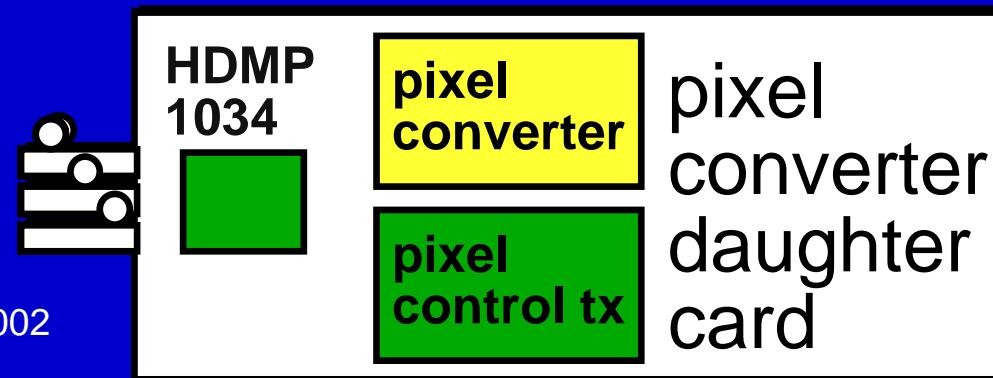
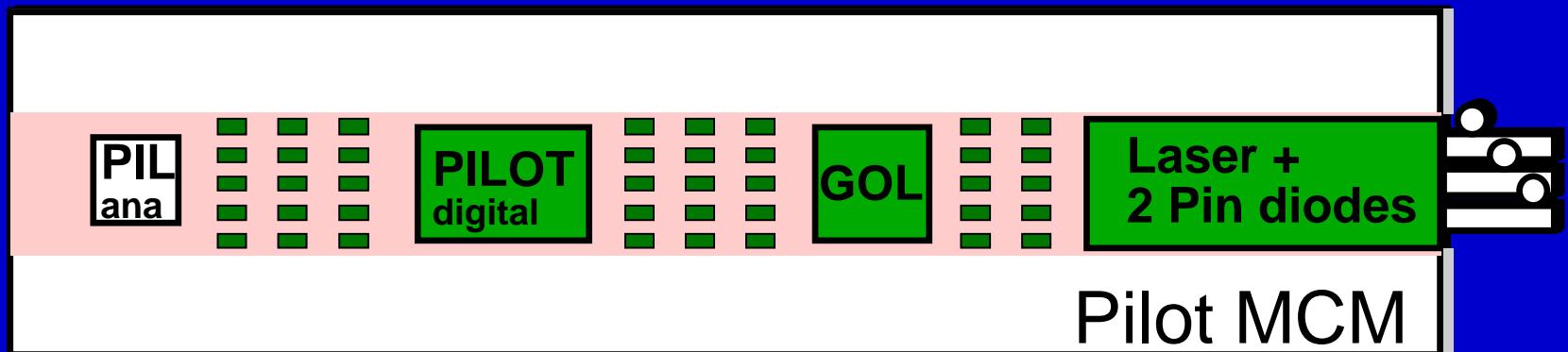
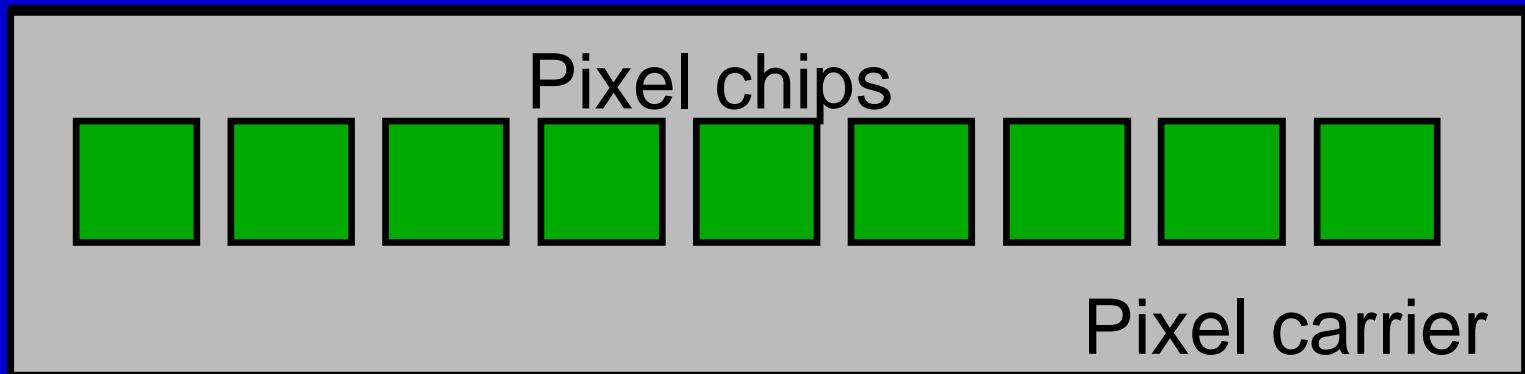
# Component Status



# Component Status



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# Conclusion

- Structured on detector read-out architecture
- Hard physical implementation constraints
- Prototypes exist but not the final versions
- Positive Progress